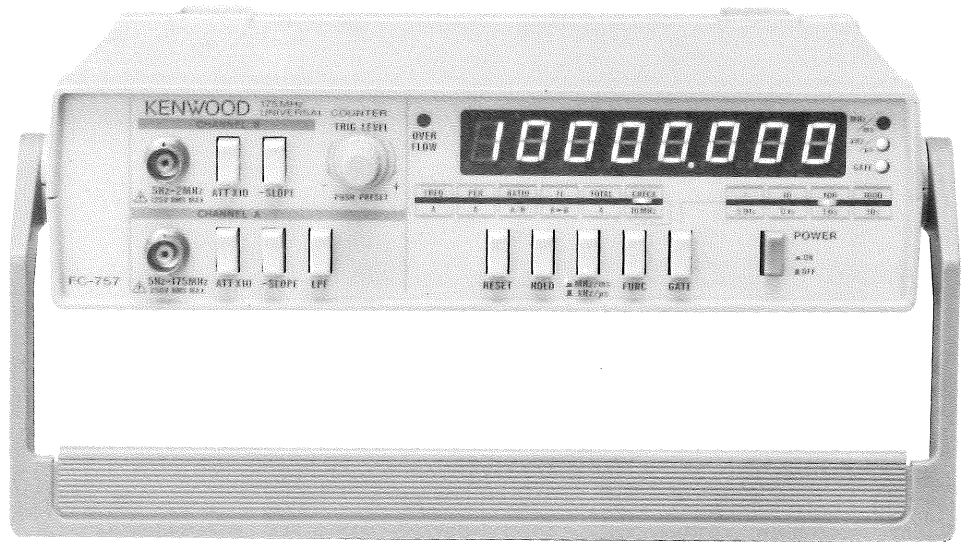


175MHz UNIVERSAL COUNTER

# FC-757

## SERVICE MANUAL

KENWOOD CORPORATION



KENWOOD

## **WARNING**

The following instructions are for use by qualified personnel only. To avoid electric shock, do not perform any servicing other than contained in the operating instructions unless you are qualified to do so.

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# SPECIFICATION

<b>FC-757</b>	
<b>Frequency Measurement (Channel A)</b>	
Measurement range	kHz mode: 5 Hz to 10 MHz MHz mode: 5 Hz to 175 MHz
Accuracy	± Reference time accuracy ± 1 count
Resolution	kHz mode: 0.1 Hz to 100 Hz MHz mode: 1 Hz to 1000 Hz
Counting time (Gate time)	kHz: 0.01s, 0.1s, 1.0s, 10s MHz: 0.02s, 0.2s, 2.0s, 20s
Unit	kHz, MHz
<b>Period Measurement (A)</b>	
Measurement range	0.5 μs to 200 ms (5 Hz to 2 MHz)
Accuracy	± 1 count ± reference time accuracy ± trigger error *1
Resolution	100 ps to 100 ns
Unit	ms, μs
Minimum pulse width	250 ns
Magnification (Gate time)	× 1, × 10, × 100, × 1000
<b>Frequency Ratio Measurement (A/B)</b>	
Measurement range A	5 Hz to 10 MHz
Measurement range B	5 Hz to 2 MHz
Denominator magnification	Denominator magnification N: × 1, × 10, × 100, × 1000
Accuracy	$\pm \left( \frac{\text{Freq B}}{\text{Freq A} \times N} \right) \pm \text{Trigger error}$ N: magnification
<b>Time Interval Measurement (A to B)</b>	
Measurement range	0.5 μs to 200 ms (5 Hz to 2 MHz)
Resolution	100 ps to 100 ns
Accuracy	± 1 count ± Reference time accuracy ± Trigger error ± N
Minimum pulse width (A to B)	250 ns
Unit	ms, μs
Magnification	× 1, × 10, × 100, × 1000
Single-shot pulse processing	Wait by reset
<b>Event input Total Measurement (A)</b>	
Measurement range	5 Hz to 10 MHz
Maximum total count	0 to 99,999,999
Control	Reset/Hold control from the front panel. Always active except for the case where the Start/Stop input terminal level is 'InActive (active high).
<b>Input Characteristics (channel A)</b>	
Frequency band width	5 Hz to 175 MHz (Coupling: AC coupling)
Sensitivity (sine wave)	kHz mode: 20mVr.m.s. (5 Hz to 10 MHz) MHz mode: 50mVr.m.s. (5 MHz to 125 MHz) 100mVr.m.s. (125 MHz to 150 MHz) 150mVr.m.s. (150 MHz to 175 MHz)
Impedance	1.2 MΩ, 40 pF or less
Maximum input voltage	250Vr.m.s. at (5 Hz to 50 Hz)

# SPECIFICATION

<b>FC-757</b>	
Attenuation	× 1 (1/1), × 10 (1/10)
Low pass filter	10 kHz, - 3 dB
slope	+/- selectable
Trigger level	Presetable or variable (about ± 1 V)
<b>Input Characteristics (Channel B)</b>	
Frequency band width	5 Hz to 2 MHz (Coupling : AC coupling)
Sensitivity (sine wave)	30mVr.m.s.
Impedance	1.2 MΩ, 40 pF or less
Maximum input voltage	125Vr.m.s. at (5 Hz to 60 Hz)
Attenuation	× 1 (1/1), × 10 (1/10)
Slope	+/- selectable
<b>Reference Oscillator</b>	
Oscillation frequency	10.0 MHz (5 Hz to 175 MHz)
Stabilization (Temperature factor, aging rate)	3 × 10 <sup>-6</sup> /° to 40°C 5 × 10 <sup>-7</sup> /month
<b>Reference Frequency Input</b>	
Frequency	10 MHz
Input sensitivity	1.77Vr.m.s. or less
Coupling	AC
Input impedance	540 Ω
<b>Display Function</b>	
Display	Eight-digit LED display kHz/μs, MHz/ms, GATE, OVER FLOW
Functions display	FREQ, PER, RATIO, TI (A to B), TOTAL, CHECK
Counting time (Gate time)	0.01s, 0.1s, 1.0s, 10s 1, 10, 100, 1000
<b>Self-check Function</b>	
Display	Display a count value of the internal time base timer (10.0 MHz)
Counting time (Gate time)	0.01s, 0.1s, 1.0s, 10s
Resolution	0.1 Hz to 100 Hz
<b>General Requirements</b>	
Power supply voltage	100/120/220/240 VAC ± 10% (max. 250 V), 50/60 Hz
Power consumption	20 VA
Within specifications temperature and humidity	23°C ± 5°C, 70%RH
Operating temperature and humidity	0°C to 40°C, 80%RH
Dimensions	240(W) × 64(H) × 190(D) mm [max. 260(W) × 70(H) × 210(D) mm]
Weight	1.8 kg
Accessories	Instruction manual 1 Power supply cable 1 Replacement fuse 1

\*1 Trigger error is typically ± 0.3% of reading divided by the number of cycles averaged, for input signals having better than 40 dB S/N ratio and greater than 100 mV amplitude.



# SAFETY

## SAFETY

Before connecting the instrument to a power source, carefully read the following information, then verify that the proper power cord is used and the proper line fuse is installed for power source. The specified voltage is shown nearby at the AC inlet. If the power cord is not applied for specified voltage, there is always a certain amount of danger from electric shock.

### Line voltage

This instrument operates using ac-power input voltages that 100/120/220/240 V at frequencies from 50 Hz to 60 Hz.

### Power cord

The ground wire of the 3-wire ac power plug places the chassis and housing of the instrument at earth ground. Do not attempt to defeat the ground wire connection or float the instrument; to do so may pose a great safety hazard.

The appropriate power cord is supplied by an option that is specified when the instrument is ordered.

The optional power cords are shown as follows in Fig. 1.

### Line fuse

The fuse holder is located on the rear panel and contains the line fuse. Verify that the proper fuse is installed by replacing the line fuse.

### Voltage conversion

This instrument may be operated from a 100 V to 240 V, 50/60 Hz power source. Use the following procedure to change from 100 to 240 volt operation or vice versa.

1. Remove the fuse holder.
2. Replace fuse F 5 with a fuse of appropriate value, 0.25 amp for 100 VAC to 120 VAC operation, 0.125 amp for 220 VAC to 240 VAC operation.
3. Reinsert it for appropriate voltage range.
4. When performing the reinsertion of fuse holder for the voltage conversion, the appropriate power cord should be used. (See Fig. 1.)







Plug configuration	Power cord and plug type	Factory installed instrument fuse	Line cord plug fuse	Parts No. for power cord and plate
	North American 120 volt/60 Hz Rated 15 amp (12 amp max; NEC)	0.25 A, 250 V Slow blow 6 × 30 mm	None	Cord: E30-1820-05
	Universal Europe 220 volt/50 Hz Rated 16 amp	0.125 A, 250 V Slow blow 6 × 30 mm	None	Cord: E30-1819-05
	U.K. 240 volt/50 Hz Rated 13 amp	0.125 A, 250 V Slow blow 6 × 30 mm	0.8 A Type C	—
	Australian 240 volt/50 Hz Rated 10 amp	0.125 A, 250 V Slow blow 6 × 30 mm	None	Cord: E30-1821-05
	North American 240 volt/60 Hz Rated 15 amp (12 amp max; NEC)	0.125 A, 250 V Slow blow 6 × 30 mm	None	—
	Switzerland 240 volt/50 Hz Rated 10 amp	0.125 A, 250 V Slow blow 6 × 30 mm	None	—

Fig. 1 Power Input Voltage Configuration

# CIRCUIT DESCRIPTION

This discussion can best be followed by referring to the separately supplied schematic diagrams, and to the accompanying figures when directed by the text. The discussion is separated into major sections corresponding to those depicted in the main block diagram.

## Channel A Input Buffer

Refer to the schematic diagram. The input signal is capacitively coupled via R101 and C101 to the divider of R102 and R103. X10 switch S7 selects either the full voltage across the divider or only the portion across R103 (approximately one tenth of the full amount). The signal is level-clamped to a maximum of  $\pm 1.2$  volts by Transistor Q101, Q102, Q116 and Q117 it is then applied to the high-impedance buffer stage consisting of Q103, used as a source follower, and Q104, which serves as a current sink and enhances response to negative signal excursions. Transistor Q105 is used as a current source for successive stages.

## Channel A Filter

The signal is applied to the low-pass filter consisting of R112, R113 and C116, whose values set a  $-3$  dB point of approximately 10 kHz. When FILTER switch S9 is pushed in (ON position on schematic), diodes D106 and D107, are biased on. This provides an ac path to ground through D107 and the filter action of R112, R113 and C116 is enabled. When S9 is released, D106 and D107 are off, isolating C116 from ground, and disabling the filter action.

## Channel A Preamplifier

The differential amplifier of transistor array IC101 compares the input signal to a variable dc level from the TRIG LEVEL control, R124. When TRIG LEVEL is pushed in (PRESET-IN), S13 is closed, bringing the amplifier input at IC101 pin 4 to approximately ground potential. The other input, at pin 1, is taken from the output of the filter. This signal, capacitively coupled at the counter input by C101, experiences no dc offset in the buffer or filter stages. Therefore, when applied to pin 1 of IC101, its average level remains near ground potential. As a result, when TRIG LEVEL is set to PRESET-IN, the quiescent level of the differential amp is set at approximately the average level of the input. When TRIG LEVEL is pulled out, S13 is opened, and the pin 4 input level is controlled by R124, which varies the quiescent level above or below the input average.

## Channel A Amplifier

This stage (IC102) amplifies and shapes the input to ultimately produce a digital waveform which is suitable for use in the counting circuits. The circuit makes use of a 10216 ECL triple line receiver for good response throughout the frequency range of the instrument. Third of the amps in this IC are used to square up the signal.

The chip supplies a voltage reference of 3.8 volts at pin 11. this is applied through R128-R130 and R148 to the

inputs of the first amp (pins 9 and 10). A quiescent voltage difference of approximately 5 millivolts results between the two inputs. This defines the minimum amount of signal required at these inputs for proper "squaring" to occur.

The second amp, at PIN 4 and 5, is used as a amplifier which "squaring" the input signal. The third amp, at pins 12 and 13 is used to provide further "squaring" of the waveform. Inputs to this amp are the complementary outputs of the second amp.

Transistors Q106 and Q107 are used as ECL-to-TTL level shifters. The waveform obtained across R141 is a 0 to 2.8 volt square wave with the same polarity as the input signal.

## Channel B Input Buffer

The Channel B input signal is capacitively coupled via C140 to the divider of R151 and R152. X10 switch S10 selects either the full voltage across the divider or only the portion across R152 (approximately one tenth of the full amount). The signal is level-clamped to a maximum of  $\pm 1.2$  volts by Transistor Q110, Q111, Q118, Q119 and applied to the high-impedance buffer stage. This consists of FET Q112, which provides high input impedance and unity gain, and Q113, which serves as a current source for successive stages.

## Channel B Amplifier/Schmitt Trigger

This stage (IC105) operates in a similar manner to its Channel A counterpart (IC102), to square the waveform for use in the counter circuits. As in Channel B, a 10116 ECL triple line receiver (IC105) is used. The first two amps shown on the schematic are used for squaring, and the third serves as the Schmitt trigger.

The  $+5.0$  V voltage is applied through R157, R174 and R175 to the input of the first amp (pins 9 and 10), defining the minimum squaring level (about 5 mV). The complementary outputs are applied to the second amp at pins 4 and 5 for further squaring of the waveform. The Schmitt trigger at pins 12 and 13 provides a noise margin; its trigger threshold is obtained from the pin 11 reference via R168 and R169 determines the amount of hysteresis. Transistors Q114 and Q115 are the ECL-to-TTL level shifters. The R172 waveform is a 0-2.8 volt square wave with the same polarity as the input.

# CIRCUIT DESCRIPTION

## Channel A/Channel B Slope Select

Positive or negative trigger slope is selected by applying the inputs through EXCLUSIVE-OR gates U18 pins 8-13. The other input to each gate is set either high or low by the -SL (slope) switch. The result is that either the signal or its complement is fed through to U20.

## Channel A Signal Gating

The Channel A signal from U15 pin 8 is EXCLUSIVE-OR in U18 (pins 11, 12, 13) with the output of the HOLD flip-flop (U1 and HOLD switch S3) and the voltage from the TOTALIZE START/STOP jack on the rear panel. This permits the input to be gated, either manually or electronically, during the TOTALize mode. When no control signal is connected to TOTALize jack the jack is pulled high by R27.

## Time Interval Priming Circuit

Before any Time Interval measurement, U20 must be primed by a high-to-low transition of input A, followed by a similar transition of input B. In cases of repetitive input waveforms, the chip is automatically primed. However, for instances where one (and only one) time interval is to be measured, a priming circuit is used.

The circuit consists of three NAND gate from U8, two EXCLUSIVE-OR's of U18, two NAND gate of U1, and RESET switch S1. The input signals, lines are fed through the XOR's. Most of the time the other XOR inputs (from the priming circuit) are low.

However, when preparing to time a single event, lines U18 pin 11 and U18 pin 8 are a stable high (because the input should be stable in anticipation of the event). Pressing RESET takes U18 pin 4 high also (only, however, if TI mode is selected, enabling NAND gate U1 ). This produces a low at U18 pin 6. When RESET is released at U18 pin 6 goes back high, and the inverters at U8 pins 1-3 and 11-13 produce a momentary low at U18 pin 3. After this priming sequence of each XOR going low and high, the priming circuit resumes its steady state conditions, and the AND gate outputs follow U18 pin 8 and U18 pin 11 for the time interval measurement.

## Channel A Prescaler

Maximum guaranteed operating frequency of the counter chip, U20, is 10 MHz. To extend the frequency range to 150 MHz, the counter employs a prescaler consisting of two frequency dividers in the Channel A digital input path. The first is a divide-by-ten, IC103, whose input is taken from the output of the Channel A amplifier at IC102 pin 15. This is immediately followed by U19, a divide-by-two.

The output of U19 is applied to a circuit consisting of the four NAND gates of U16 and U17, which select either the frequency-divided signal or the original-frequency signal from the priming circuit. The selection circuit is governed by the

output of U15 pin 6, which goes high only during FREQ MHz mode (also discussed in the paragraphs on "Counter Circuits" below). Whenever this mode is selected, the frequency-divided version is applied to the counter circuits.

The effect of the divide-by-two operation on the input is compensated for by another divide-by-two, U19, connected between pins 38 and 33 of the ICM7226A. As explained in the "Counter Circuits" paragraphs, whenever FREQ MHz mode is enabled, this circuit divides the counter time base by two.

The effect of the divide-by-ten on the input is compensated by shifting of the display decimal point, also discussed in the "Counter Circuits" paragraphs.

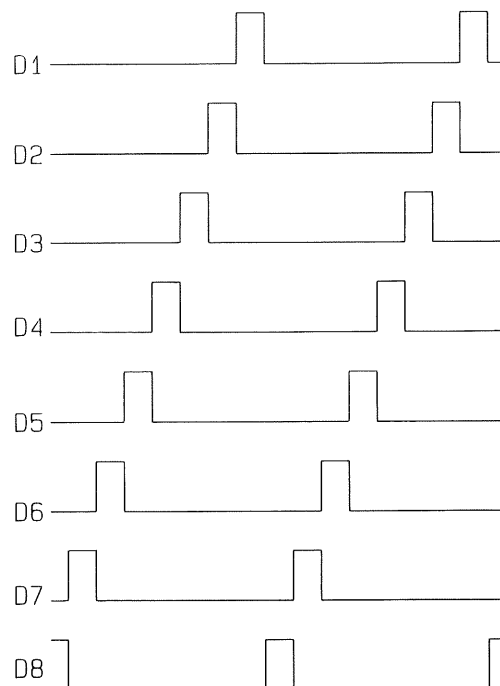
## ICM7226A Counter

This integrated circuit, U20, is the heart of the unit. It performs all counting functions and multiplexes and drives the displays. It requires an input signal of digital logic levels, as provided by the circuits previously discussed. A TCXO for the time base oscillator is also required, as well as external connections for feedback of display digit strobes, as described below.

## Digit Strokes and Feedback

The 7226A multiplexes the display by means of digit strobes D1-D8. Each strobe goes high in sequence, as in fig. 2, turning its display digit on momentarily. As each digit is selected, the proper seven-segment and decimal point information for that digit is sent out at the same time on pins 8-11 and 13-16.

Fig. 2 U20 digit strobes



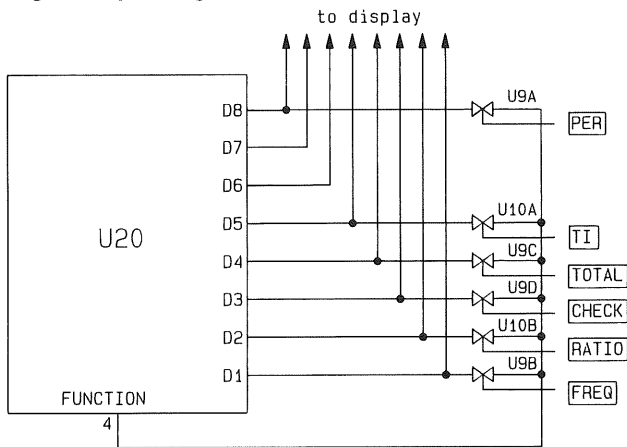
# CIRCUIT DESCRIPTION

The digit strobes D1-D8 are also used to control the 7226A by selective feedback to four control pins, 1, 4, 20, and 21. Operating mode, resolution, and other parameters are determined by which strobe signal is present at each control input. Strobe feedback is controlled by the front panel settings, either directly or through logic. Each control pin and its feedback network is discussed below.

## Operating Mode Selection

Operating mode selection is controlled by FUNCTION pin 4. As shown in fig. 3, this pin is directly connected to one of digit strobes D1-D5 or D8 via bilateral switches U9 and U10.

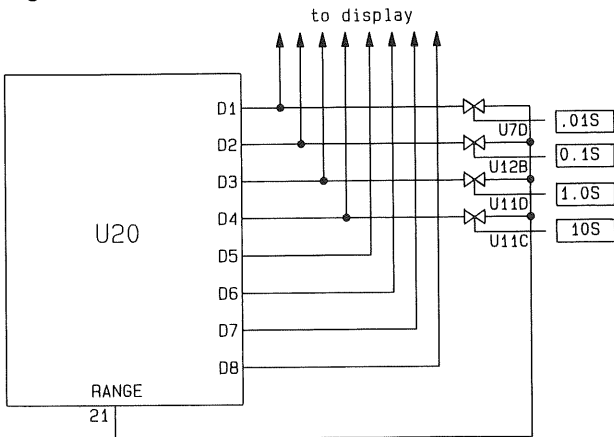
Fig. 3 Operating mode selection



## Resolution Selection

Resolution selection is controlled by RANGE pin 21. As shown in fig. 4, digit strobes D1-D4 are applied directly to pin 21 via bilateral switches U7, U11 and U12.

Fig. 4 Resolution selection



## Additional Control-pin 1

Additional control of U20 is provided by feedback of strobes D1, D3, and D8 to CONTROL pin 1. This feedback is determined by the front panel function setting as shown in Fig. 5. In Fig. 5 these outputs are used to gate the strobes to pin 1 via bilateral switches U13 which provide a low resistance path from input to output when energized.

D8 is applied whenever the 10s Gate time bilateral switch U11 is engaged, the K/u-M/m switch is pushed in, and PERiod, Time Interval, or CHECK mode is selected. U20 responds by outputting the "Display Test" condition, causing the display to read all eights and decimal points.

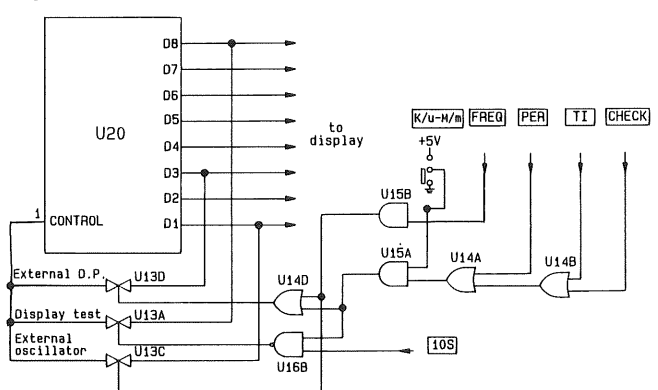
D1 is gated whenever the unit is in FREQ MHz mode. This instructs U20 to use the signal at pin 33 as a time base. This is merely the output of a divide-by-two circuit whose input is the regular 10 MHz time base (made available at pin 38). Thus, whenever FREQ MHz mode is used, the time base is divided by two. This divider is included to compensate for the previously discussed divide-by-two used in the input path.

D3 is applied whenever any of the conditions listed in page 10 are true. This instructs U20 to use external decimal point control, as explained in the next section.

## External Decimal Point

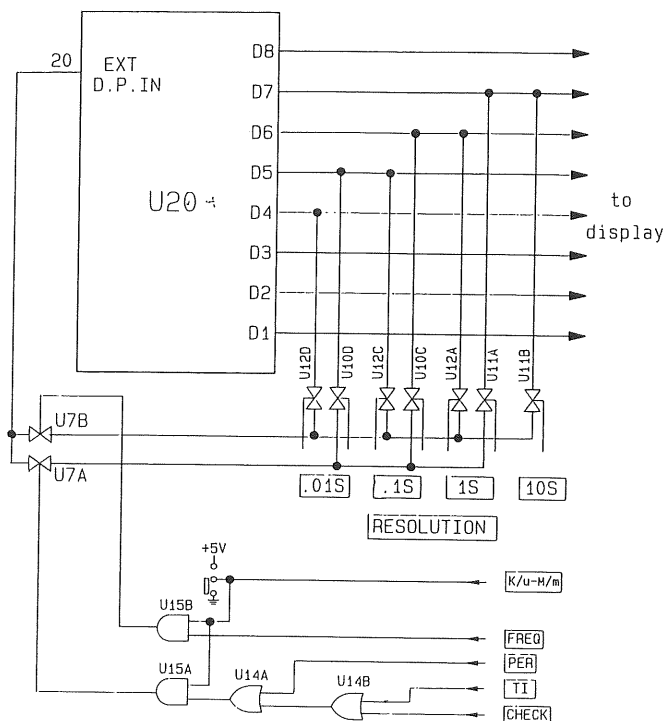
External decimal point placement is enabled in all of the modes listed in fig. 5. When D3 is applied to pin 1, the 7226A disables automatic selection, and places a decimal point at the display digit whose strobe is applied to pin 20, EXT DP IN. As shown in fig. 6 that position is determined partially by the Gate time switches, and partially by the particular operating mode being used.

Fig. 5 Additional strobe feedback; U20 pin 1



# CIRCUIT DESCRIPTION

**Fig. 6 External decimal point control**



## Time Base

The counter employ a internal 10 MHz TCXO (temperature-compensated crystal Oscillator) and External Time Base Amplifies circuit via slide switch (S12) selected. For increased temperature stability. As shown on the schematic diagram, the TCXO is connected to the Oscillator input of U20 via U21 External Time Base which amplifies the EXT. Input signal only 10 MHz to a level suitable for driving U20 via U21.

## HOLD Switch

Refer to the schematic diagram. The HOLD switch, S2, is connected via U1, which provides switch debouche, to U20 and U15. The connection to U20 instructs the chip to enter the display HOLD mode whenever the switch is engaged, In TOTALize operation, however, U20 would freeze only the display but keep on counting; this is remedied by also connecting S2 to U15. This cuts off the input from U20 (as does a low at the TOTALIZE START/STOP jack) and halts the counting process.

## LED Indicators

The MHz/ms and KHz/us indicators are connected to complementary signals which are a direct function of the setting of S3, the K/u, M/m switch. They are, however, disabled when U14 pin 8 goes high, in RATIO and TOTALize modes.

The GATE indicator, D26, is connected via inverter U5 (pins 9 and 10) to U20 pin 3. This pin goes low whenever

a measurement is in progress.

The FREQ, PER, RATIO, TI, TOTAL, CHECK indicator (LED1-LED6) is connected via U4 PIN 2-7, PIN 9-12 and PIN 14-15, U4 Buffers the output of U2, the gate time indicators are driven by U5 which is connected to U3 output.

## Power Supply

The transformer is a universal type whose primary windings may be rewired for various line voltages by rear panel line voltage selection switch S14 and S15.

The output of the secondary side is rectified by bridge D4-D7 and filtered by C10 and C11. Zener diode D10, D11, D13 and D14 provide regulated + 10, - 10, + 6.2 and - 6.2 volts, respectively.

The secondary output is also rectified by D8 and D9 and filtered by C12. + 5 volts is produced by Q1 which provide good regulation and adequate power for the digital portion of the instrument.

# BLOCK DIAGRAM

## Analog Input Circuits

These circuits process the analog input signals in preparation for the digital circuits which follow. Input buffers provide the high impedance desired, and also selectable X10 input attenuators. The Channel A signal is passed through a selectable low pass filter and a preamplifier which increases sensitivity and provides selectable preset or adjustable trigger level control. Signals from both channels are squared by amplifier/Schmitt trigger circuits, so that digital waveforms of appropriate levels are obtained.

## Digital Input Circuits

These circuits process the now-digital signals before they reach the counter circuits. The Channel A signal follows two different paths, according to function settings. In one case, it is applied to a divide-by-twenty prescaler which increases the frequency range of the unit. The other path channels to a slope selector, which chooses either the signal or its complement (the Channel B signal encounters a similar circuit), and a gating circuit which either passes or blocks it in response to a control input and a switch. This Channel A signal is then applied, together with Channel B, to the Time Interval priming circuit which passes both signals unchanged (except for special instances in Time Interval mode).

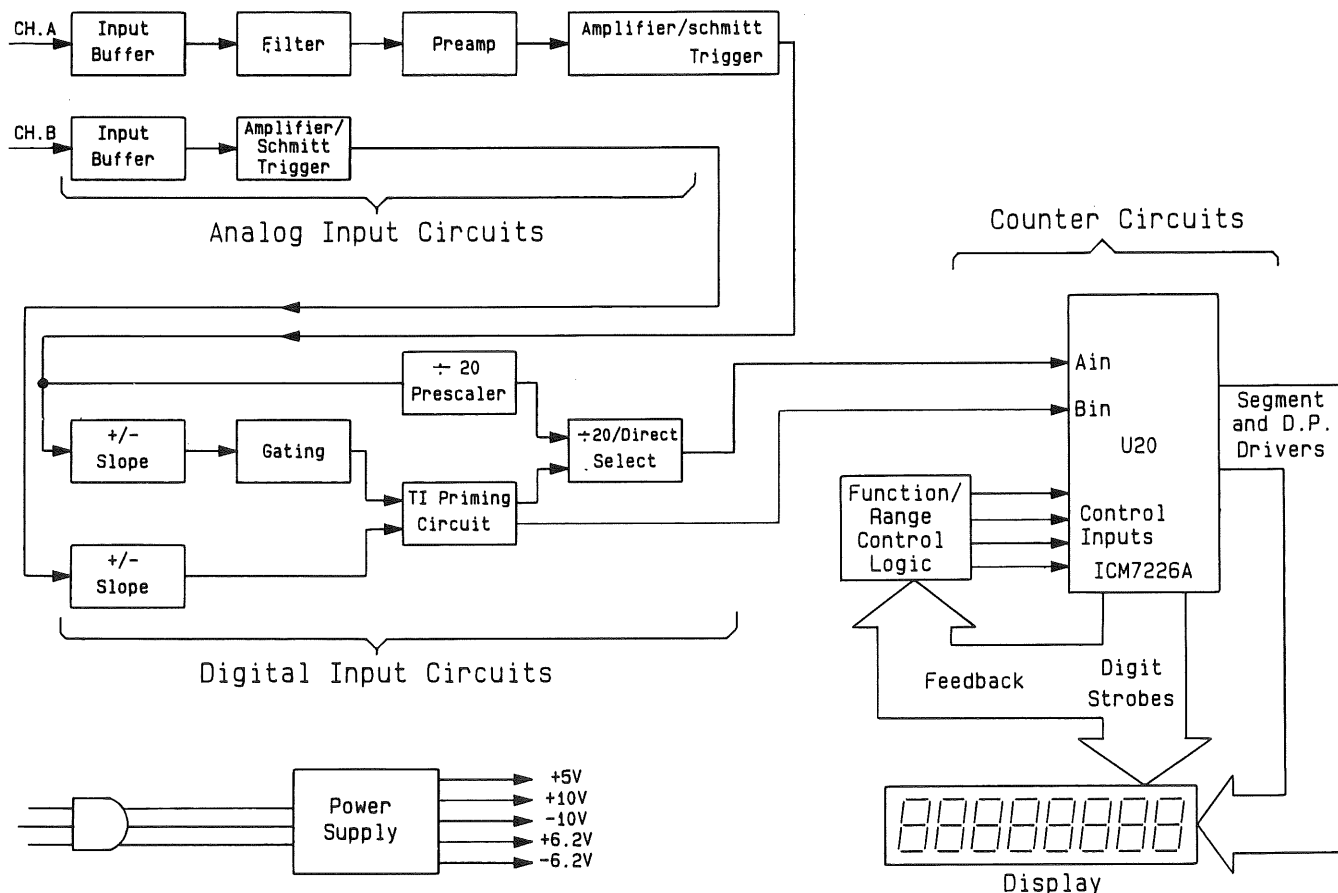
The two Channel A paths converge in a selection circuit which chooses either the original frequency or the divided-down version, in accordance with operating mode selected. This signal and that from Channel B are applied to the counter circuits.

## Counter Circuits

These center around an ICM7226A Universal Counter integrated circuit, which performs all counting functions. Four control signals to the chip determine operating mode and other factors. They themselves are derived as feed back from the chip's own digit strobes (which are used as multiplex signals for the display); the feed back is selected by the front panel switches via the control logic.

## Power Supply

The power supply provides regulated voltages as shown. The tapped, dual-primary transformer is universal, and can be selected as needed for various line voltages.



# ADJUSTMENT

## 1. TCXO Time Base

The model utilize a temperature-compensated crystal oscillator for exceptional temperature stability. Because of the high accuracy of the TCXO, a 10 MHz standard of accuracy at least 1 part in 10000000 is required for calibration. However, if a proper frequency standard is available, calibration is accomplished as follows,

- a. With power disconnected, remove the rubber seal from the top case.
- b. Reconnect power to the unit, warm up for at least 30 minutes.
- c. Connect a 10 MHz frequency standard of accuracy at least 1 part in 10000000 to the channel A input jack. Select FREQUENCY kHz mode and 1 sec gate time.
- d. Using a non-metallic alignment tool, adjust through the time base adjust hole of the top case and the hole of the TCXO shield for display 10000,000.
- e. Disconnect power and replace rubber seal.

### Note:

- \* The top case should be removed when proceed the following procedures.
- \*\* Disconnect the ac power before remove the screws of the top case, then reconnect the ac power when top case has been removed.
- \*\*\* Disconnect the ac power and replace the top cover when finished the following procedures.

## 2. Channel A sensitivity

- a. Connect a 175 MHz, 100 mV RMS sinewave signal to channel A input.
- b. Set the counter's TRIG LEVEL control to preset in position.
- c. Set the channel A ATT switch and LPF switch out.
- d. Adjust R130 on main PCB for the correct readings.
- e. Reduce the input signal and slightly readjust R130 for correct readings.
- f. Repeat step "e" until get the best sensitivity.

## 3. Channel A Trigger Level

- a. Disconnect the unit from AC power, remove the screws and top case.
- b. Reconnect power to the unit, warm up for at least 30 minutes.
- c. Push the counter's TRIG LEVEL control into PRESET in position.
- d. Pull the counter's TRIG LEVEL out and rotate it fully clockwise.
- e. Connect a 10 kHz/1.4 V RMS sinewave signal to the channel A input and set the counter to the FREQUENCY MHz mode with 1.0 s gate time range.
- f. Set R147 fully counter-clockwise, then, adjust R125 for a display reading of 10 KHz.

- g. Reduce the input signal level by 0.1 V RMS and readjust R125 for 10 kHz display reading in both clockwise and counter-clockwise TRIG LEVEL settings.
- h. Continue the step "h", until no further adjustment is possible.
- i. Set the input sinewave signal to 1.1 V RMS, rotate the TRIG LEVEL VR. fully counter-clockwise.
- j. Readjust R147 until the display again reads 10 kHz.
- k. Turn the TRIG LEVEL control fully CW. The display should still read 10 kHz. If not, repeat the previous four steps until the display reads 10 kHz in both fully CW and CCW TRIG LEVEL control settings.

## 4. Channel B T.I. Adjust

- a. Set counter at T.I. Mode.
- b. Connect a 5 Hz, 80 mV squarewave to Channel A and B input.
- c. Adjust R175 for correct reading at the slope condition  $A+/B-$ ,  $A+/B+$ ,  $A-/B-$ ,  $A-/B+$ .

## 5. Channel B Frequency Ratio A/B Adjust

- a. Set counter at F.R. Mode.
- b. Applying a 10 MHz, 50 mV sinewave at Channel A input and a 2 MHz, 30 mV sinewave at Channel B input.
- c. Adjust R179 for correct reading.

# TROUBLESHOOTING

The following troubleshooting steps provide a logical procedure for fault isolation. While the procedure can not, of course, guarantee to pinpoint every possible problem, it will in most cases localize the problem to a certain area.

Most of these troubleshooting steps require removal of the top cover as described previously.

The separately supplied schematic diagram should also be consulted in conjunction with this procedure. Finally, it should be mentioned that some insight into troubleshooting the unit may be gained by studying the CIRCUIT DESCRIPTION section of this manual.

1. Set PWR to ON and connect a 1 MHz signal source to both inputs. Frequency accuracy of the source is not critical; however, amplitude should be adequate to produce stable counter readings. Use the input controls (filter, attenuator, trigger, slope and level) as necessary to obtain a stable readout. (if a stable reading cannot be obtained, follow step 5.)
2. Set the counter to each of the settings of Table. 1 and check that the display shows approximately the values listed. If it does not, proceed as follows:
  - a. If no display can be obtained, follow step 3.
  - b. If display shows abnormalities such as missing decimal points or unlit segments or digits, follow step 4.
  - c. If display appears normal, but value is incorrect or unstable, follow step 5.
  - d. If problem is not adequately described by any of the above, start at step 3 and proceed through each step until the difficulty is isolated.
3. No Display: Check supply voltage at U20 pin 25 for approximately +5 V.  
If this voltage is not present, check ac input, fuse, and +5 V power supply circuit (D8, D9, C12, Q1). Otherwise proceed to step 4.
4. Abnormal Display
  - a. **Digit Strokes and Time Base**  
Check for the digit strobe waveforms of Fig. 7 at U20 pin 22-24 and 26-30. If these are normal, proceed to step 4 b. If not, check the output of the time base oscillator at pin 38 for an approximate sine wave of frequency 10 MHz and peaks of 0 and 2 V. If normal, proceed to step 4b; if no output is obtained, check oscillator components TCXO and U20.
  - b. **Display Test**  
Engage the 10s Gate time switch and select CHECK mode. Display should be all "eights" with all decimal points and OVERFLOW indicator on. If not, switch to PERIOD and Time Interval modes (same RESOLUTION) and check for same display in each. If the self test display appears in one mode and not in another, check mode selection circuitry as in step 5j. If it does not appear in any modes, or is incorrect in all modes, check the seven-segment displays and U20 segment driver pins 8-11 and 13-16. Waveform at each of these pins should approximate a dc level of about 1.2 V, with negative spikes of about 4 kHz.
  - c. **Decimal Points**  
If these are abnormal in MHz or ms modes, check the mode selection logic as in step 5 j (particularly Table 7).
  - d. **kHz/us or MHz/ms Indicators**  
For the problems involving these, check the mode selection logic as in step 5 j (particularly Table 8).
  - e. **GATE Indicator**  
This LED, D26 is connected via U5 PIN 9, 10 to U20 pin 3, which goes low whenever a measurement is being taken.  
Check D26, U5 pin 9,10 and U20 pin 3. (If pin 3 shows no activity, it is advisable to check for proper mode selection as in step 5j)
  - f. **Function Indicator**  
If the Function indicator FREQ, PER, RATIO, TI, TOTAL and CHECK LED, LED 1-LED 6, does not function properly check LED 1-LED 6, U4 and U2.
  - g. **Gate Time Indicator**  
If the Gate time indicator 0.01s, 0.1s, 1.0s and 10s LED, LED 7-LED 10 does not function properly check LED 7-LED 10, U5 and U3.
5. Incorrect or Unstable Display Value
  - a. **Isolation by Half-Splitting**  
Check the waveform at the collector of Q106 (Channel A) and Q115 (Channel B). With a 1 MHz input to each counter channel, each of these waveforms should be a 1 MHz square wave (0-2.4 V) of same polarity as the channel input. If either waveform is abnormal, a problem may exist in the analog input circuitry for that channel; see steps 5b & 5c. Otherwise, troubleshoot the digital circuitry; see steps 5d to 5j.
  - b. **Analog Circuitry Power Supply**  
Check for voltages of +6, -6, +10, and -10 volt in the analog circuits (appropriate points are shown on the amplifier board schematic). If these voltages are



# TROUBLESHOOTING

not present, check power supply (D4-7, D10, D11, D13, D14, C10, C11 and Fuse 1-2).

## c. Analog Input Circuits

Tables 2 & 3 give waveforms for the analog input circuits for Channel A and Channel B respectively (using a 10 kHz, 1 V p-p sinusoidal input). The order of table entries is from input to output; this permits either sequential or half-splitting troubleshooting techniques, as desired by the user.

## d. Slope Select Gates

With the Channel A -SL switch S8 out, the TTL waveform at U18 pin 11 should be of the opposite polarity as that at the collector of Q106 (see step 5a above). Pushing the switch in should complement the signal. Similarly, the waveform at U18 pin 8 should be opposite to that at the collector of Q115 except when complemented by the Channel B -SL switch. If either waveform is abnormal, check U18 and the -SL switches.

## e. Channel A Gating

Check waveform at U15 pin 8 TTL waveform should be the same as that at U18 pin 11. S3 in (or applying a TTL low signal at TOTALIZE START/STOP jack) should result in a constant low at U15 pin 8. If waveform is abnormal, check U15, S3, U16, or TOTALIZE input network.

## f. TI Priming Circuit

Check waveforms at U18 pins 6 and 3 (Channels A and B, respectively). With RESET switch out, waveforms should be the same as those at U15 pin 8 and U18 pin 8, respectively. If not, check the priming circuit and RESET switch S1 as in Table 4.

Also consult this table if the unit fails to properly perform single time interval measurements.

## g. Prescaler

Set counter input to 1 MHz, and check frequency of waveforms at IC103 pin 4 (should be 100 kHz, non-symmetrical waveform) and U19 pin 9; (should be 50 kHz, symmetrical waveform). If either is abnormal, check IC103 or U19.

## h. Prescale/Direct Selection Circuit

For a 1 MHz counter input, the waveform at U17 pin 8 should also be 1 MHz when FREQ kHz mode is selected. When FREQ MHz is selected, the frequency at U17 pin 8 should be 50 kHz. If the waveform is abnormal, check that U16 pin 12, 13 is high when FREQ MHz is selected. If not, check the mode selection logic as in step 5j (particularly Table 8). Otherwise, check the gates of U16 and U17.

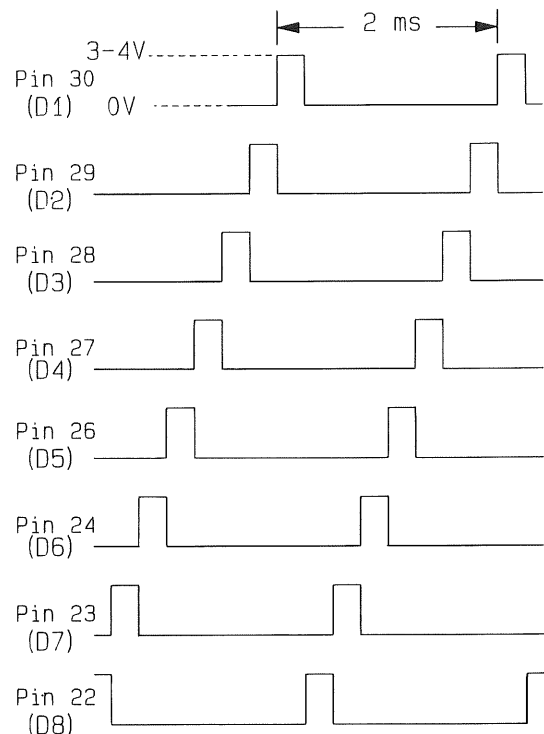
## i. Time Base Divider

The waveform at U19 pin 5 should be 1/2 of the frequency of that at U19 pin 3 (10 MHz time base from U20). If not, check U19.

## j. Mode Selection Logic

Operating mode, resolution, and other factors are determined by feedback of the U20 digit strobes D1-D8 to various control pins of this same chip. This feedback is controlled, either directly or through logic, by the front panel switches. Tables 5-8 give normal logic conditions in these feedback connections for each switch configuration.

Fig. 7 Digit strobe waveform from U20



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**TABLE 1** Normal display for 1 MHz input

Operating Mode	GATE TIME	Ideal Display
FREQuency kHz	0.01s	1000.0
	0.1s	1000.00
	1.0s	1000.000
	10s	1000.0000*
FREQuency MHz	0.01s	1.000
	0.1s	1.0000
	1.0s	1.00000
	10s	1.000000**
PERiod us	0.01s	1.0
	0.1s	1.00
	1.0s	1.000
	10s	1.0000
PERiod ms	0.01s	.0010
	0.1s	.00100
	1.0s	.001000
	10s	Display test***
RATIO	0.01s	1.
	0.1s	1.0
	1.0s	1.00
	10s	1.000
TI us (both -SL switches out, TRIG LEVEL set to PRESER IN)	0.01s	1.0
	0.1s	1.00
	1.0s	1.000
	10s	1.0000
TI ms (both -SL switches out, TRIG LEVEL set to PRESET IN)	0.01s	.0010
	0.1s	.00100
	1.0s	.001000
	10s	Display test***
TOTALize	not applicable.	Display accumulates, with second digit from left changing at approximately 1 Hz
PERiod (Reduce input to less than 100 Hz)	10s	OVERflow lights.*

\* Allow ten seconds for measurement completion.

\*\* Allow twenty seconds for measurement completion.

\*\*\* Display all eights, all decimal points and OVERflow LED light.

**TABLE 2** Channel A analog circuit waveform

Test Point	Waveform
A. Gate of Q103	1Vp-p/10 kHz sine wave, centered at 0 V.
B. Gate of Q103 (Ch.A X10 switch engaged)	0.1Vp-p/10 kHz sine wave, centered at 0 V.
C. Base of Q105.	1Vp-p/10 kHz sine wave, centered at +1.2 V.
D. IC101 pin 1 (LPF SW out)	0.9Vp-p/10 kHz sine wave, centered at 0 V, in phase with input.
E. IC101 pin 1 (LPF SW in)	10 kHz sine wave, approx. 0.5Vp-p, centered at 0 V, shift by approx. 45° behind input.
F. IC101 pin 4	With TRIG LEVEL pulled out and rotated, voltage at pin 4 should vary from -1.2 V to +1.2 V. (0 V with TRIG LEVEL pushed in)
G. IC101 pin 13 (TRIG LEVEL pushed in)	10 kHz 0.6Vp-p, rounded square wave, centered at 5.0 V. Rotation of TRIGGER LEVEL should have no effect.
H. IC101 pin 13 (TRIG LEVEL pulled out)	With TRIG LEVEL pulled out and centered, waveform is same as G. Rotating the control counter-clockwise increases the duty cycle toward a dc level of +6 V at extreme rotation; clockwise rotation decreases the duty cycle toward a dc level of +4 V at extreme rotation.
I. IC102 pin 11 (input disconnected)	DC level of +3.8 V.
J. IC102 pin 9, 10 (input disconnected)	Same as I.
K. IC102 pin 10 (input reconnected)	0.6Vp-p/10 kHz rounded square wave, centered at +3.8 V.
L. IC102 pin 7, 5	1Vp-p/10 kHz square wave, centered at +3.8 V. Polarity opposite that of J; squarer edges.
M. IC102 pin 2, 6, 13, 15, and base of Q106	Same as L, but inverted.
N. IC102 pin 3, 12, 14, and base of Q107	Same as L.

Note: Channel A input of 1 V p-p, 10 kHz sine wave.

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**Table 3** Channel B analog circuit waveform

Test Points	Waveforms
A. Gate of Q112	1Vp-p/10 kHz sinewave, centered at 0 V.
B. Gate of Q112 (CH.B X10 switch engaged)	0.1Vp-p/10 kHz sinewave, centered at 0 V.
C. Base of Q113	1Vp-p/10 kHz sinewave, centered at +2.3 V.
D. IC105 pin 11 (input disconnected)	DC level of +3.8 V.
E. IC105 pin 9 (input disconnected)	DC level of +3.0 V.
F. IC105 pin 10 (input disconnected)	Same as E.
G. IC105 pin 10 (input reconnected)	0.4Vp-p/10 kHz sinewave, centered at +2.8 V.
H. IC105 pins 7, 4	1Vp-p/10 kHz rounded square wave, at centered +3.8 V.
I. IC105 pins 5, 6	Same as H, but inverted.
J. IC105 pins 2, 13, 15	Same as I, with squarer corners.
K. IC105 pin 14	Same as J, but inverted.
L. Base of Q114, Q115	1Vp-p/10 kHz square wave, but polarity are inverted.

Note: Channel B input of 1 V p-p, 10 kHz sine wave.

**Table 4** Check of T.I. priming circuit

Function Setting	Test Points	Waveforms
TI mode engaged, RESET switch out	U1 pin 1, 2, 11, 13	Logic high
	U1 pin 3, 12	Logic low
Press/Release RESET	U8 pin 3, 6, 8, 11	Logic low
	U8 pin 1, 2, 4, 5, 9, 10, 12, 13	Logic high
	U18 pin 3	Same as U18 pin 2
	U18 pin 6	Same as U18 pin 5
Press/Release RESET	U18 pin 4 should goes high as long as RESET is held down. Upon release of the button, U18 pin 4 returns low, followed by a brief high (5 ms) at U18 pin 1.	

**Table 5** Check of gate time

Gate Engaged	Test Points	Waveform
0.01s Gate time	U20 pin 21	U20 strobe D1 (pin 30)
	U7 pin 4	U20 strobe D4 (pin 27)
	U7 pin 1	U20 strobe D5 (pin 26)
0.1s Gate time	U20 pin 21	U20 strobe D2 (pin 29)
	U7 pin 4	U20 strobe D5 (pin 26)
	U7 pin 1	U20 strobe D6 (pin 24)
1.0s Gate time	U20 pin 21	U20 strobe D3 (pin 28)
	U7 pin 4	U20 strobe D6 (pin 24)
	U7 pin 1	U20 strobe D7 (pin 23)
10s Gate time	U20 pin 21	U20 strobe D4 (pin 27)
	U7 pin 4	U20 strobe D7 (pin 23)

**Table 6** Check of Function and related logic

Function Engaged	Test Points	Waveform
FREquency A	U20 pin 4 U18 pin 12	U20 strobe D1 (pin 30) Logic high
PERiod A	U20 pin 4 U14 pins 2 U15 pin 1	U20 strobe D8 (pin 22) Logic high Logic high
RATIO A/B	U20 pin 4 U14 pins 8, 9 cathodes of D24, D25	U20 strobe D2 (pin 29) Logic high
TI A to B	U20 pin 4 U14 pins (1, 3, 4, 6) U15 pin 1 U1 pin 13	U20 strobe D5 (pin 26) Logic high Logic high Logic high
TOTALize A	U20 pin 4 U14 pin 8, 10 cathodes of D24, D25	U20 strobe D4 (pin 27) Logic high
CHECK	U20 pin 4 U14 pins (1, 3, 5, 6) U15 pin 1	U20 strobe D3 (pin 28) Logic high Logic high

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**Table 7** Check of External decimal point enable

Function Engaged	Test Points	Waveform
K/u-M/m, FREQuency A	U15 pins 5, 6, 3 U7 pin 5 U7 pin 3, and U20 pin 20  U14 pins 11, 12 U13 pin 12 U13 pin 10  U20 pin 1	Logic high Logic high Same as U7 pin 4 (U20 digit strobe selected by function; see Table 5) Logic high Logic high U20 strobe D3 (pin 28) U20 strobe D1 (pin 30) and strobe D3 (pin 28)
K/u-M/m, PERiod, T1 and CHECK	U14 pin 3  U15 pins 1, 12 U7 pin 13 U7 pin 2, and U20 pin 20  U14 pins 11, 13 U13 pin 12 U13 pin 10  U20 pin 1	Logic high (see Table 6) Logic high LOgic high Same as U7 pin 1 (U20 digit selected by Gate time switches; see Table 5) Logic high Logic high U20 strobe D3 (pin 28) U20 strobe D3 (pin 28)

**Table 8** Additional checks of function selection logic

Function Engaged	Test Points	Waveform
K/u-M/m, FREQuency A	U17 pin 13 & U1 pin 4, 8 U13 pin 8 and U20 pin 1	Logic high Same as U13 pin 9 (U20 strobe D1, D3)
K/u-M/m, 10s Gate time, PERi- od, T1 or CHECK	U14 pin 3 & U15 pin 1, 12 U16 pin 1, 2 U16 pin 3 U13 pin 2 and U20 pin 1	Logic high Logic high Logic low Same as U13 pin 1 (U20 strobe D8 and D3)
K/u-M/m engaged (no others)	U14 pin 8 & U5 pin 12 U5 pin 11 & anode of D24 Anode of D25 D24 D25	Logic low Logic high Logic low Lit Unlit
K/u-M/m disengaged	U14 pin 8, U5 pin 11 Anode of D24 U5 pin 12 & anode of D25 D24 D25	Logic low Logic low Logic high Unlit Lit



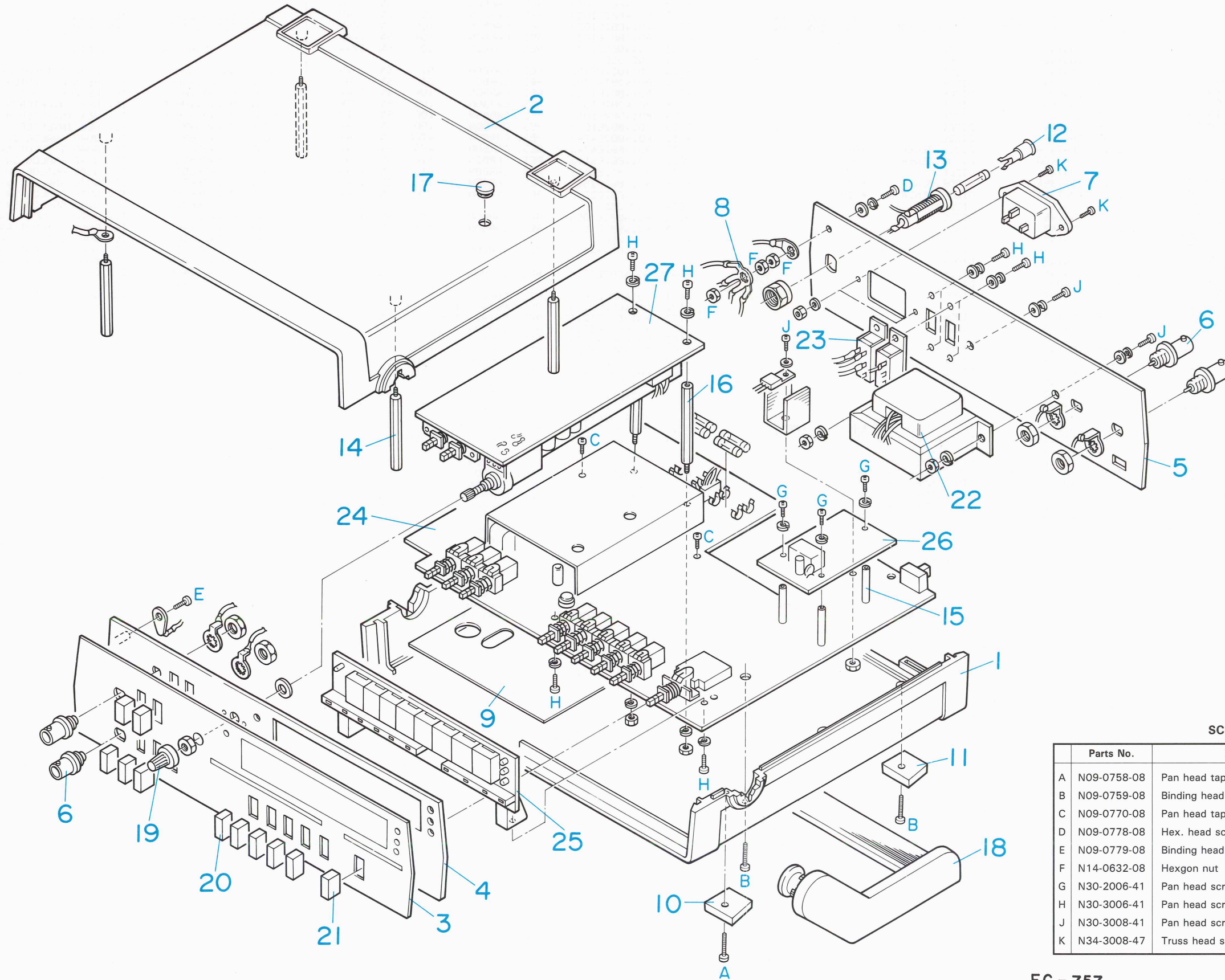
# PARTS LIST

## FC-757 UNIT

(Y81-1050-00)

REF. NO	PARTS NO	NAME & DESCRIPTION
	B41-0870-08	FUSE CAUTION LABEL
	B42-3693-08	SERIAL LABEL
	B50-7725-00	INSTRUCTION MANUAL, JAPANESE
	B50-7726-00	INSTRUCTION MANUAL, ENGLISH
	E30-1644-15	BS POWER CORD
	E30-1818-05	JIS POWER CORD SET
	E30-1819-05	CEE POWER CORD
	E30-1820-05	UL/CSA POWER CORD
	E30-1821-05	SAA POWER CORD
	F51-0001-05	FUSE(SLOW BLOW) 250V 0.25A
	F51-0002-05	FUSE(SLOW BLOW) 250V 0.125A
	G02-0612-08	COIL SPRING
	H01-5912-08	CARTON BOX
	H12-0571-08	FOAMED PAD
	H20-1728-08	VIYNL COVER 320X340X0.06
1	A02-0523-08	BOTTOM CASE
2	A02-0530-08	TOP CASE
3	A21-1166-08	OVERLAY
4	A22-0880-08	FRONT PANEL
5	A23-1701-08	BACK PANEL
6	E04-0259-05	BNC RECEPTACLE
7	E18-0351-05	AC INLET 3 P
8	E22-0282-08	4 LEG LUG
9	F10-1629-08	SHIELD PAPER
10	J02-0520-08	RUBBER FOOT(FRONT)
11	J02-0521-08	RUBBER FOOT(REAR)
12	J13-0515-08	FUSE CARRIER
13	J13-0516-08	FUSE BASE
14	J32-0882-08	HEX. STUD L=44.2
15	J32-0896-08	HEX. STUD
16	J32-0897-08	HEX. STUD
17	J42-0555-08	RUBBER PLUG
18	K01-0527-08	HANDLE
19	K23-0810-08	KNOB
20	K27-0542-08	PUSH KNOB, WHITE WHITE
21	K27-0557-08	PUSH KNOB, ORANGE
22	L01-9944-08	POWER TRANSFORMER
23	S31-1510-08	SLIDE SWITCH
24	W02-0489-08	MAIN UNIT
25	W02-0490-08	DISPLAY UNIT
26	W02-0491-08	TCXD UNIT
27	W02-0492-08	CH B UNIT

# DISASSEMBLY



### SCREWS

Parts No.	Parts Name	Figure
A	N09-0758-08 Pan head tapite screw (3.5×8)	
B	N09-0759-08 Binding head screw (6/32inch×18)	
C	N09-0770-08 Pan head tapite screw (3.5×6)	
D	N09-0778-08 Hex. head screw (M3.5×6)	
E	N09-0779-08 Binding head sciew (M3.5×6)	
F	N14-0632-08 Hexgon nut (M3.5)	
G	N30-2006-41 Pan head screw (M2×6)	
H	N30-3006-41 Pan head screw (M3×6)	
J	N30-3008-41 Pan head screw (M3×8)	
K	N34-3008-47 Truss head screw (M3×8)	

# PARTS LIST

MAIN UNIT (W02-0489-08)			
REF.NO	PARTS NO	NAME & DESCRIPTION	
	E02-0155-08	IC SOCKET 14 PIN	
	E04-0259-05	BNC RECEPTACLE	
	E18-0351-05	AC INLET 3 P	
	E23-0584-08	PIN	
	E38-0001-08	WIRE ASS'Y:DISPLAY TO MAIN GND	
	E38-0006-08	WIRE ASS'Y:G151 TO CH 8 BNC	
	E38-0008-08	WIRE ASS'Y:J101 TO JE.ETC.	
	E38-0010-08	WIRE ASS'Y:JA,J8,J0 TO DISPLAY	
	E38-0011-08	WIRE ASS'Y:JC TO DISPLAY PCB	
	F01-0880-08	HEAT SINK	
	F10-1630-08	SHIELD CASE	
	J13-0514-08	FUSE CLIP	
	J73-0006-08	PCB (UNMOUNTED)	
	R92-0150-05	JUMPING RES. ZERO OHM(10MM)	
C001	CK45F1H104Z	CAP. CERAMIC 0.1 50V	
C002	CK45F1H104Z	CAP. CERAMIC 0.1 50V	
C003	CK45F1H104Z	CAP. CERAMIC 0.1 50V	
C004	CE04EW1C470M	CAP. ELECTRO 47 20% 16V	
C005	CK45F1H104Z	CAP. CERAMIC 0.1 50V	
C006	C91-1321-08	CAP. POLYESTER 0.22 10% 630V	
C007	C91-1320-08	CAP. CERAMIC 0.001 20% 4KV	
C008	C91-1320-08	CAP. CERAMIC 0.001 20% 4KV	
C009	CE04EW1C470M	CAP. ELECTRO 47 20% 16V	
C010	CE04EW1V102M	CAP. ELECTRO 1000 20% 35V	
C011	CE04EW1V102M	CAP. ELECTRO 1000 20% 35V	
C012	CE04EW1E472M	CAP. ELECTRO 4700 20% 25V	
C013		NO USE	
C014	CK45F1H104Z	CAP. CERAMIC 0.1 50V	
C015	CK45F1H104Z	CAP. CERAMIC 0.1 50V	
C016		NO USE	
C017	CK45F1H104Z	CAP. CERAMIC 0.1 50V	
C018	CK45F1H104Z	CAP. CERAMIC 0.1 50V	
C019	CK45F1H104Z	CAP. CERAMIC 0.1 50V	
C020	CK45F1H104Z	CAP. CERAMIC 0.1 50V	
C021	CK45F1H104Z	CAP. CERAMIC 0.1 50V	
C022	CK45F1H104Z	CAP. CERAMIC 0.1 50V	
C023	CK45F1H104Z	CAP. CERAMIC 0.1 50V	
C024	CK45F1H104Z	CAP. CERAMIC 0.1 50V	
C025	CK45F1H104Z	CAP. CERAMIC 0.1 50V	
C026	CK45F1H104Z	CAP. CERAMIC 0.1 50V	
C027	CK45F1H104Z	CAP. CERAMIC 0.1 50V	
C028	CC45SL1H221J	CAP. CERAMIC 220P 5% 50V	
C029	CC45CH2H390J	CAP. CERAMIC 39P 5% 500V	
C033	CK45F1H104Z	CAP. CERAMIC 0.1 50V	
C034	CK45B2H102K	CAP. CERAMIC 1000P 10% 500V	
C038	CE04EW1C470M	CAP. ELECTRO 47 20% 16V	
C101	CF93AN2G474K	CAP. POLYESTER 0.47 10% 400V	
C102	CC45CH2H010C	CAP. CERAMIC 1P 0.25P 500V	
C103	CC45CH2H120J	CAP. CERAMIC 12P 5% 500V	
C104	CM93BF2H131J	CAP. MICA 130P 5% 500V	
C105	CK45B1H103K	CAP. CERAMIC 0.01 10% 50V	
C106	CK45B1H103K	CAP. CERAMIC 0.01 10% 50V	
C107	CK45B1H103K	CAP. CERAMIC 0.01 10% 50V	
C108	CK45B1H103K	CAP. CERAMIC 0.01 10% 50V	
C109	CK45B1H103K	CAP. CERAMIC 0.01 10% 50V	
C110	CK45B1H103K	CAP. CERAMIC 0.01 10% 50V	
C111	CC45CH2A620J	CAP. CERAMIC 62P 5% 100V	
C112	CE04EW1C470M	CAP. ELECTRO 47 20% 16V	
C113	CK45B1H103K	CAP. CERAMIC 0.01 10% 50V	
C114	CK45B1H103K	CAP. CERAMIC 0.01 10% 50V	
C115	CK45B2H101K	CAP. CERAMIC 100P 10% 500V	
C116	C91-1322-08	CAP. MULTILAYER 0.1 10% 50V	
C117	CE04EW1J3R3M	CAP. ELECTRO 3.3 20% 63V	
C118	CE04EW1A221M	CAP. ELECTRO 220 20% 10V	
C119	CE04EW1A221M	CAP. ELECTRO 220 20% 10V	
C120	CK45B1H103K	CAP. CERAMIC 0.01 10% 50V	
C121	CK45B1H103K	CAP. CERAMIC 0.01 10% 50V	
C122	CK45B1H103K	CAP. CERAMIC 0.01 10% 50V	
C123	CK45B1H103K	CAP. CERAMIC 0.01 10% 50V	
C124	CE04EW1A221M	CAP. ELECTRO 220 20% 10V	
C125	CK45B1H103K	CAP. CERAMIC 0.01 10% 50V	
C126	CE04EW1C470M	CAP. ELECTRO 47 20% 16V	
C127	CK45B1H103K	CAP. CERAMIC 0.01 10% 50V	
C128	CK45B1H103K	CAP. CERAMIC 0.01 10% 50V	
C129	CK45B2H102K	CAP. CERAMIC 1000P 10% 500V	
C130	CK45B1H103K	CAP. CERAMIC 0.01 10% 50V	
C131	CK45B2H102K	CAP. CERAMIC 1000P 10% 500V	
C132	CE04EW1C471M	CAP. ELECTRO 470 20% 16V	
C133	CE04EW1C471M	CAP. ELECTRO 470 20% 16V	
C134	CE04EW1J3R3M	CAP. ELECTRO 3.3 20% 63V	

REF.NO	PARTS NO	NAME & DESCRIPTION	
C135	CE04EW1J3R3M	CAP. ELECTRO 3.3 20% 63V	
C136	CC45SL1H471J	CAP. CERAMIC 470P 5% 50V	
C152	CE04EW1A221M	CAP. ELECTRO 220 20% 10V	
C153	CE04EW1A221M	CAP. ELECTRO 220 20% 10V	
D001	1N4148	DIODE	
D002	1N4148	DIODE	
D003	1N4148	DIODE	
D004	1N4004	DIODE	
D005	1N4004	DIODE	
D006	1N4004	DIODE	
D007	1N4004	DIODE	
D008	1N4004	DIODE	
D009	1N4004	DIODE	
D010	1N4740A	DIODE.ZENER 10V	
D011	1N4740A	DIODE.ZENER 10V	
D012	1N4148	DIODE	
D013	1N4735A	DIODE.ZENER 6.2V	
D014	1N4735A	DIODE.ZENER 6.2V	
D015	1N4148	DIODE	
D016	1N4148	DIODE	
D017	1N4148	DIODE	
D018	1N4148	DIODE	
D019	1N4148	DIODE	
D020	1N4148	DIODE	
D021	1N4148	DIODE	
D022	1N4007	DIODE	
D023	1N4007	DIODE	
D028	1N4148	DIODE	
D029	1N4148	DIODE	
D103	1N4148	DIODE	
D104	1N4148	DIODE	
D105	1N4148	DIODE	
D106	1N4148	DIODE	
D107	1N4148	DIODE	
D108	1N4148	DIODE	
IC101	CA3102E	IC. DUAL HF DIFFERENTIAL AMP	
IC102	MC10216P	IC. TRIPLE LINE RECEIVER	
IC103	SP8660	IC. COUNTER	
JA	E40-7103-08	PIN CONNECTOR 8P	
JB	E40-7103-08	PIN CONNECTOR 8P	
JC	E40-7104-08	PIN CONNECTOR 9P	
JD	E40-7103-08	PIN CONNECTOR 8P	
J101	E40-7106-08	PIN CONNECTOR 4P	
J102	E40-7106-08	PIN CONNECTOR 4P	
J106	E40-7107-08	PIN CONNECTOR 6P	
J110	E40-7108-08	PIN CONNECTOR 2P	
L001	L39-0532-08	COIL	
Q001	MC7805CT	IC. POSITIVE VOLTAGE REGULATOR	
Q002	2N2369	TR. SI. NPN	
Q003	MC7805CT	IC. POSITIVE VOLTAGE REGULATOR	
Q101	2SC1674(K)	TR. SI. NPN	
Q102	2SC1674(K)	TR. SI. NPN	
Q103	2N5486	FET. N-CHANNEL	
Q104	2N5486	FET. N-CHANNEL	
Q105	2SC535(C)	TR. SI. NPN	
Q106	MPS3640	TR. SI. PNP	
Q107	MPS3640	TR. SI. PNP	
Q108	2N5486	FET. N-CHANNEL	
Q109	2SC1815(GR)	TR. SI. NPN	
Q116	2SC1674(K)	TR. SI. NPN	
Q117	2SC1674(K)	TR. SI. NPN	
R001	RD14BB2E103J	RES. CARBON 10K 5% 1/4W	
R002	RD14BB2E103J	RES. CARBON 10K 5% 1/4W	
R003	RD14BB2E474J	RES. CARBON 470K 5% 1/4W	
R004	RD14BB2E103J	RES. CARBON 10K 5% 1/4W	
R005	RD14BB2E103J	RES. CARBON 10K 5% 1/4W	
R006	RD14BB2E474J	RES. CARBON 470K 5% 1/4W	
R007	RD14BB2E104J	RES. CARBON 100K 5% 1/4W	
R008	RD14BB2E102J	RES. CARBON 1K 5% 1/4W	
R009	RD14BB2E104J	RES. CARBON 100K 5% 1/4W	
R010	RD14BB2E104J	RES. CARBON 100K 5% 1/4W	
R011	RD14BB2E104J	RES. CARBON 100K 5% 1/4W	
R014	RD14BB2E181J	RES. CARBON 180 5% 1/4W	
R015	RD14BB2E471J	RES. CARBON 470 5% 1/4W	
R016	RD14BB2E181J	RES. CARBON 180 5% 1/4W	
R017	RD14BB2E471J	RES. CARBON 470 5% 1/4W	
R018	RD14BB2E103J	RES. CARBON 10K 5% 1/4W	
R019	RD14BB2E103J	RES. CARBON 10K 5% 1/4W	
R020	RD14BB2E103J	RES. CARBON 10K 5% 1/4W	
R021	RD14BB2E103J	RES. CARBON 10K 5% 1/4W	
R022	RD14BB2E103J	RES. CARBON 10K 5% 1/4W	
R023	RD14BB2E103J	RES. CARBON 10K 5% 1/4W	
R024		NO USE	
R025	RD140B2H510J	RES. CARBON 51 5% 1/2W	
R026	RD140B3A330J	RES. CARBON 33 5% 1W	
R027	RD14BB2E103J	RES. CARBON 10K 5% 1/4W	
R028	RD140B2H101J	RES. CARBON 100 5% 1/2W	
R029	RD140B2H101J	RES. CARBON 100 5% 1/2W	
R030	RD14BB2E101J	RES. CARBON 100 5% 1/4W	
R031	RD14BB2E474J	RES. CARBON 470K 5% 1/4W	
R032	RD14BB2E474J	RES. CARBON 470K 5% 1/4W	
R033	RD14BB2E511J	RES. CARBON 510 5% 1/4W	
R034	RD14BB2E511J	RES. CARBON 510 5% 1/4W	
R035	RD14BB2E105J	RES. CARBON 1M 5% 1/4W	
R036	RD14BB2E221J	RES. CARBON 220 5% 1/4W	
R037		NO USE	
R038	RD14BB2E105J	RES. CARBON 1M 5% 1/4W	
R039	RD14BB2E152J	RES. CARBON 1.5K 5% 1/4W	
R040		NO USE	
R041	RD14BB2E472J	RES. CARBON 4.7K 5% 1/4W	
R045	RD14BB2E221J	RES. CARBON 220 5% 1/4W	
R101	RD14BB2E5R1J	RES. CARBON 5.1 5% 1/4W	
R102	RN14BK2E1104F	RES. METAL FILM 1.1M 1% 1/4W	
R103	RN14BK2E1213F	RES. METAL FILM 121K 1% 1/4W	
R104	RD140B3A330J	RES. CARBON 33 5% 1W	
R105	RD140B3A103J	RES. CARBON 10K 5% 1W	
R106	RD14BB2E822J	RES. CARBON 8.2K 5% 1/4W	
R107	RD14BB2E331J	RES. CARBON 330 5% 1/4W	
R108	RD14BB2E511J	RES. CARBON 510 5% 1/4W	
R109	RD14BB2E822J	RES. CARBON 8.2K 5% 1/4W	
R110	RD14BB2E101J	RES. CARBON 100 5% 1/4W	
R111	R12-1029-05	RES. SEMI FIXED 1K B	
R112	RD14BB2E121J	RES. CARBON 120 5% 1/4W	
R113	RD14BB2E330J	RES. CARBON 33 5% 1/4W	
R114	RD14BB2E152J	RES. CARBON 1.5K 5% 1/4W	
R115	RD14BB2E471J	RES. CARBON 470 5% 1/4W	
R116	RD14BB2E510J	RES. CARBON 51 5% 1/4W	
R117	RD14BB2E472J	RES. CARBON 4.7K 5% 1/4W	
R118	RD14BB2E511J	RES. CARBON 510 5% 1/4W	
R119	RD14BB2E331J	RES. CARBON 330 5% 1/4W	
R120	RD14BB2E510J	RES. CARBON 51 5% 1/4W	
R121	RD14BB2E151J	RES. CARBON 150 5% 1/4W	
R122	RN14BK2E2671F	RES. METAL FILM 2.67K 1% 1/4W	
R123	RD14BB2E332J	RES. CARBON 3.3K 5% 1/4W	
R124		NO USE	
R125	R12-1029-05	RES. SEMI FIXED 1K B	
R126	RN14BK2E2001F	RES. METAL FILM 2K 1% 1/4W	
R127	RD14BB2E511J	RES. CARBON 510 5% 1/4W	
R128	RD14BB2E332J	RES. CARBON 3.3K 5% 1/4W	
R129	RD14BB2E332J	RES. CARBON 3.3K 5% 1/4W	
R130	R12-3041-05	RES. SEMI FIXED 10KB	
R131	RD14BB2E511J	RES. CARBON 510 5% 1/4W	
R132	RD14BB2E511J	RES. CARBON 510 5% 1/4W	
R133	RD14BB2E331J	RES. CARBON 330 5% 1/4W	
R134	RD14BB2E271J	RES. CARBON 270 5% 1/4W	
R135	RD14BB2E511J	RES. CARBON 510 5% 1/4W	
R136	RD14BB2E105J	RES. CARBON 1M 5% 1/4W	
R137	RD14BB2E472J	RES. CARBON 4.7K 5% 1/4W	
R138	RD14BB2E511J	RES. CARBON 510 5% 1/4W	
R139	RD14BB2E511J	RES. CARBON 510 5% 1/4W	
R140	RD14BB2E511J	RES. CARBON 510 5% 1/4W	
R141	RD14BB2E750J	RES. CARBON 75 5% 1/4W	
R142	RD14BB2E220J	RES. CARBON 22 5% 1/4W	
R143	RD14BB2E222J	RES. CARBON 2.2K 5% 1/4W	



# PARTS LIST

## DISPLAY UNIT (W02-0490-08)

REF. NO	PARTS NO	NAME & DESCRIPTION
	J19-1667-08	LED HOLDER
	J19-1668-08	LED HOLDER
	J73-0002-08	PCB (UNMOUNTED)
D024	B30-0976-08	LED LAMP;ORANGE
D025	B30-0976-08	LED LAMP;ORANGE
D026	B30-0976-08	LED LAMP;ORANGE
D027	B30-0976-08	LED LAMP;ORANGE
DS001	B30-0975-08	LED DISPLAY
DS002	B30-0975-08	LED DISPLAY
DS003	B30-0975-08	LED DISPLAY
DS004	B30-0975-08	LED DISPLAY
DS005	B30-0975-08	LED DISPLAY
DS006	B30-0975-08	LED DISPLAY
DS007	B30-0975-08	LED DISPLAY
DS008	B30-0975-08	LED DISPLAY
LED001	B30-0977-08	LED LAMP; SQUARE, ORANGE
LED002	B30-0977-08	LED LAMP; SQUARE, ORANGE
LED003	B30-0977-08	LED LAMP; SQUARE, ORANGE
LED004	B30-0977-08	LED LAMP; SQUARE, ORANGE
LED005	B30-0977-08	LED LAMP; SQUARE, ORANGE
LED006	B30-0977-08	LED LAMP; SQUARE, ORANGE
LED007	B30-0977-08	LED LAMP; SQUARE, ORANGE
LED008	B30-0977-08	LED LAMP; SQUARE, ORANGE
LED009	B30-0977-08	LED LAMP; SQUARE, ORANGE
LED010	B30-0977-08	LED LAMP; SQUARE, ORANGE

## TCXO UNIT (W02-0491-08)

REF. NO	PARTS NO	NAME & DESCRIPTION
	J73-0005-08	PCB (UNMOUNTED)
	L77-1040-05	CRYSTAL RESONATOR (10MHZ)
C036	CK45B2A103K	CAP. CERAMIC 0.01 10% 100V
C037	CE04EW1C470M	CAP. ELECTRO 47 20% 16V
J117	E40-7029-08	PIN CONNECTOR 3P

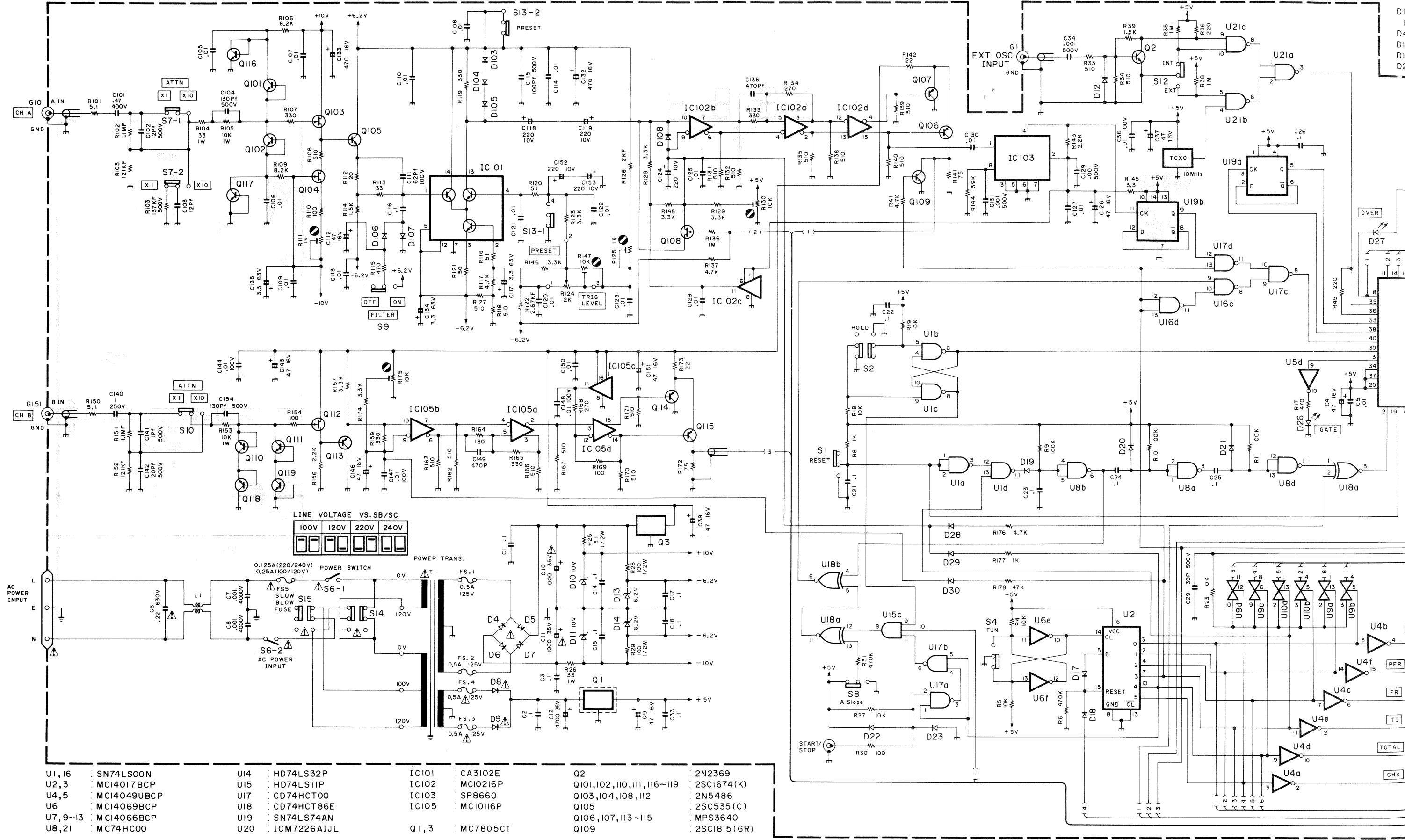
# PARTS LIST

## CHANNEL B UNIT

(W02-0492-08)

REF.NO	PARTS NO	NAME & DESCRIPTION
	E23-0584-08	PIN
	E38-0006-08	WIRE ASS'Y:G151 TO CH B BNC
	E38-0007-08	WIRE ASS'Y:G152 TO MAIN J103
	E40-7106-08	PIN CONNECTOR 4P
	F10-1633-08	SHIELD CASE
	J73-0003-08	PCB (UNMOUNTED)
	R92-0150-05	JUMPING RES. ZERO OHM(10MM)
C140	CF93AN2E105K	CAP. POLYESTER 1 10% 250V
C141	CC45CH2H010C	CAP. CERAMIC 1P 0.25P 500V
C142	CC45CH2H200J	CAP. CERAMIC 20P 5% 500V
C143	CE04EW1C470M	CAP. ELECTRO 47 20% 16V
C144	CK45B2A103K	CAP. CERAMIC 0.01 10% 100V
C145	NO USE	
C146	CE04EW1C470M	CAP. ELECTRO 47 20% 16V
C147	CK45B2A103K	CAP. CERAMIC 0.01 10% 100V
C148	CK45B2A103K	CAP. CERAMIC 0.01 10% 100V
C149	CK45B1H471J	CAP. CERAMIC 470P 5% 50V
C150	CK45B2A103K	CAP. CERAMIC 0.01 10% 100V
C151	CE04EW1C470M	CAP. ELECTRO 47 20% 16V
C154	CM93B02H131J	CAP. MICA 130P 5% 500V
D030	1N4148	DIODE
IC105	MC10116P	IC, TRIPLE LINE RECEIVER
Q110	2SC1674(K)	TR. SI, NPN
Q111	2SC1674(K)	TR. SI, NPN
Q112	2N5486	FET, N-CHANNEL
Q113	MPS3640	TR. SI, PNP
Q114	MPS3640	TR. SI, PNP
Q115	MPS3640	TR. SI, PNP
Q118	2SC1674(K)	TR. SI, NPN
Q119	2SC1674(K)	TR. SI, NPN
R124	R29-0507-08	V.R. WITH SWITCH(S13)
R146	RD14BB2E332J	RES. CARBON 3.3K 5% 1/4W
R147	R12-3041-05	RES. SEMI FIXED 10KB
R150	RD14BB2E5R1J	RES. CARBON 5.1 5% 1/4W
R151	RN14BK2E1104F	RES. METAL FILM 1.1M 1% 1/4W
R152	RN14BK2E1213F	RES. METAL FILM 121K 1% 1/4W
R153	RS14AB3A103J	RES. METAL FILM 10K 5% 1W
R154	RD14BB2E101J	RES. CARBON 100 5% 1/4W
R155	NO USE	
R156	RD14BB2E222J	RES. CARBON 2.2K 5% 1/4W
R157	RD14BB2E332J	RES. CARBON 3.3K 5% 1/4W
R158	NO USE	
R159	RD14BB2E331J	RES. CARBON 330 5% 1/4W
R162	RD14BB2E511J	RES. CARBON 510 5% 1/4W
R163	RD14BB2E511J	RES. CARBON 510 5% 1/4W
R164	RD14BB2E181J	RES. CARBON 180 5% 1/4W
R165	RD14BB2E331J	RES. CARBON 330 5% 1/4W
R166	RD14BB2E511J	RES. CARBON 510 5% 1/4W
R167	RD14BB2E511J	RES. CARBON 510 5% 1/4W
R168	RD14BB2E271J	RES. CARBON 270 5% 1/4W
R169	RD14BB2E101J	RES. CARBON 100 5% 1/4W
R170	RD14BB2E511J	RES. CARBON 510 5% 1/4W
R171	RD14BB2E511J	RES. CARBON 510 5% 1/4W
R172	RD14BB2E750J	RES. CARBON 75 5% 1/4W
R173	RD14BB2E220J	RES. CARBON 22 5% 1/4W
R174	RD14BB2E332J	RES. CARBON 3.3K 5% 1/4W
R175	R12-3041-05	RES. SEMI FIXED 10KB
R178	RD14BB2E333J	RES. CARBON 33K 5% 1/4W
S010	S42-2519-08	PUSH SWITCH

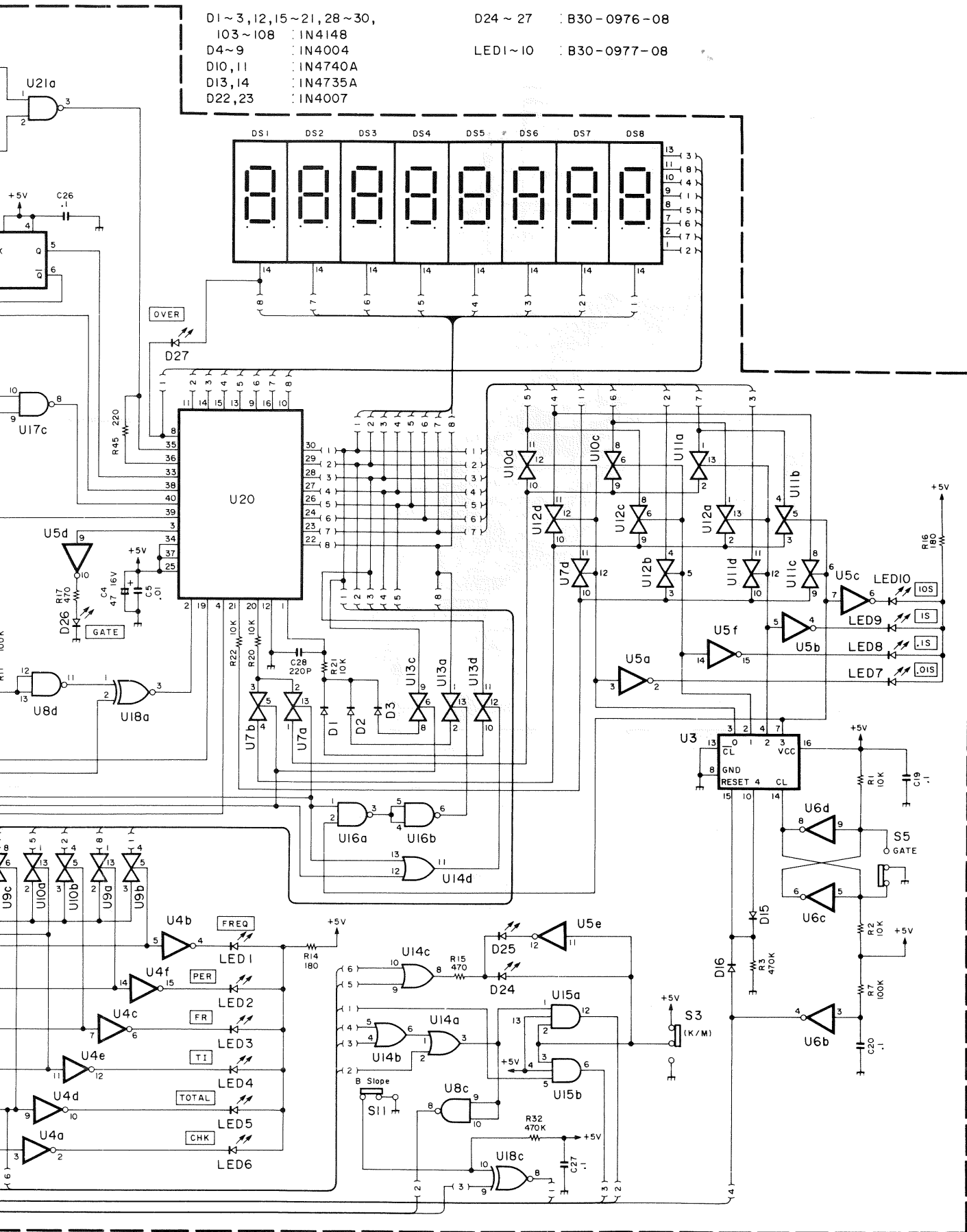
# SCHEMATIC DIAGRAM



- |                       |                   |                  |   |
|-----------------------|-------------------|------------------|---|
| U1, 16 : SN74LS00N    | U4 : HD74LS32P    | IC101 : CA3102E  | Q2 : 2N2369                               |
| U2, 3 : MC14017BCP    | U5 : HD74LS11P    | IC102 : MC10216P | Q101, 102, 110, 111, 116~119 : 2SC1674(K) |
| U4, 5 : MC14049UBCP   | U7 : CD74HCT00    | IC103 : SP8660   | Q103, 104, 108, 112 : 2N5486              |
| U6 : MC14069BCP       | U8 : CD74HCT86E   | IC105 : MC10116P | Q105 : 2SC535(C)                          |
| U7, 9~13 : MC14066BCP | U9 : SN74LS74AN   | Q1, 3 : MC7805CT | Q106, 107, 113~115 : MPS3640              |
| U8, 21 : MC74HC00     | U20 : ICM7226A1JL |                  | Q109 : 2SC1815(GR)                        |

D1 ~ 3, 12, 15 ~ 21, 28 ~ 30,  
 103 ~ 108 : IN4148  
 D4 ~ 9 : IN4004  
 D10, 11 : IN4740A  
 D13, 14 : IN4735A  
 D22, 23 : IN4007

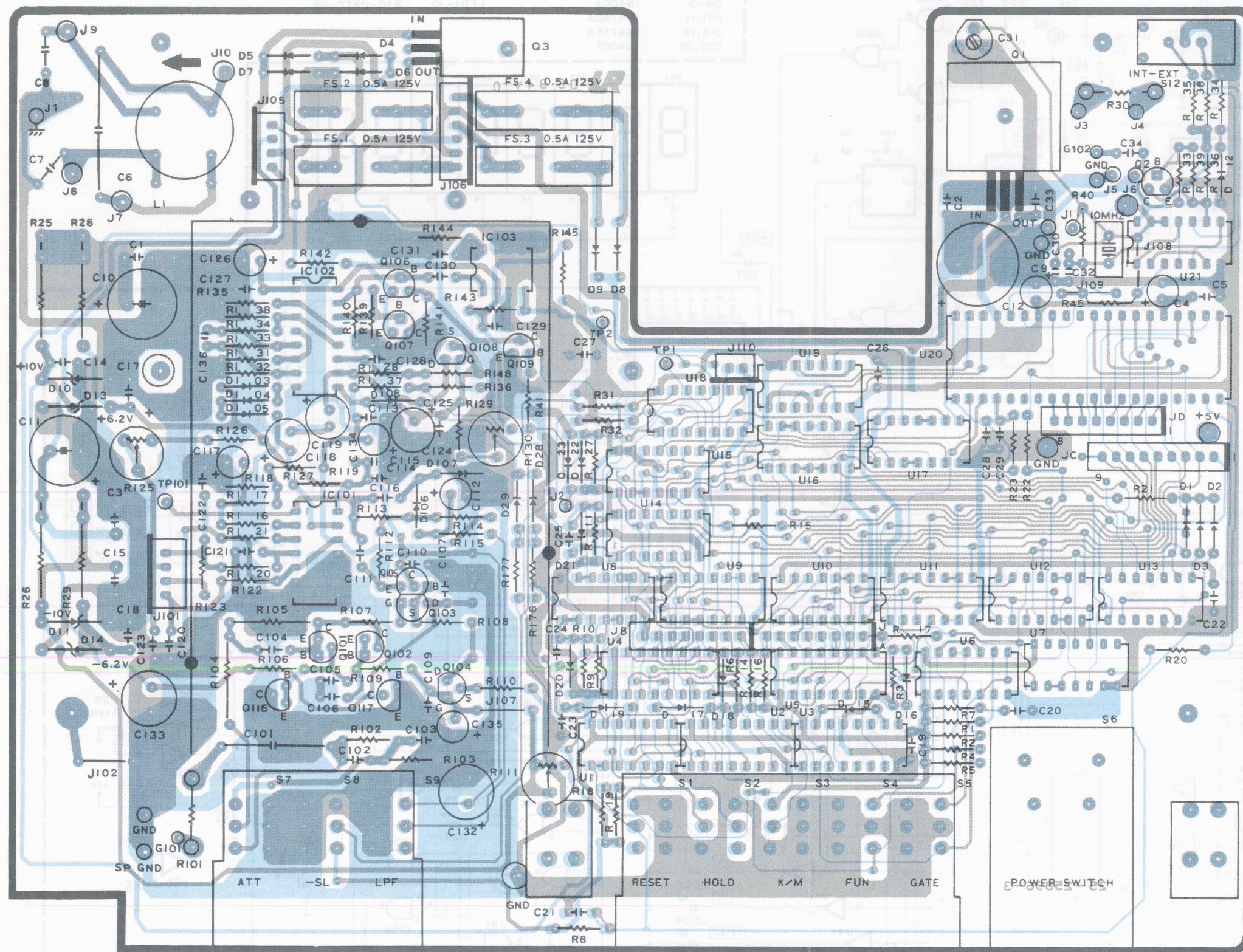
D24 ~ 27 : B30-0976-08  
 LED1 ~ 10 : B30-0977-08



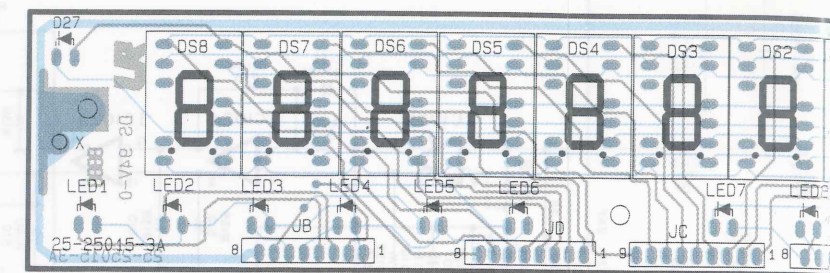


# P.C. BOARD

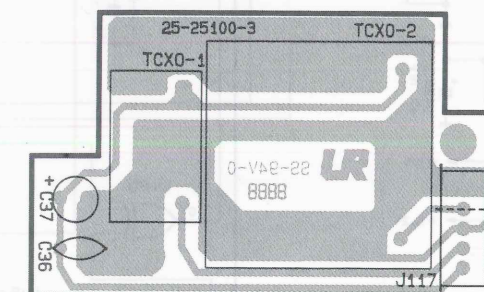
## MAIN UNIT (W02-0489-08)



## DISPLAY UNIT (W02-0490-08)

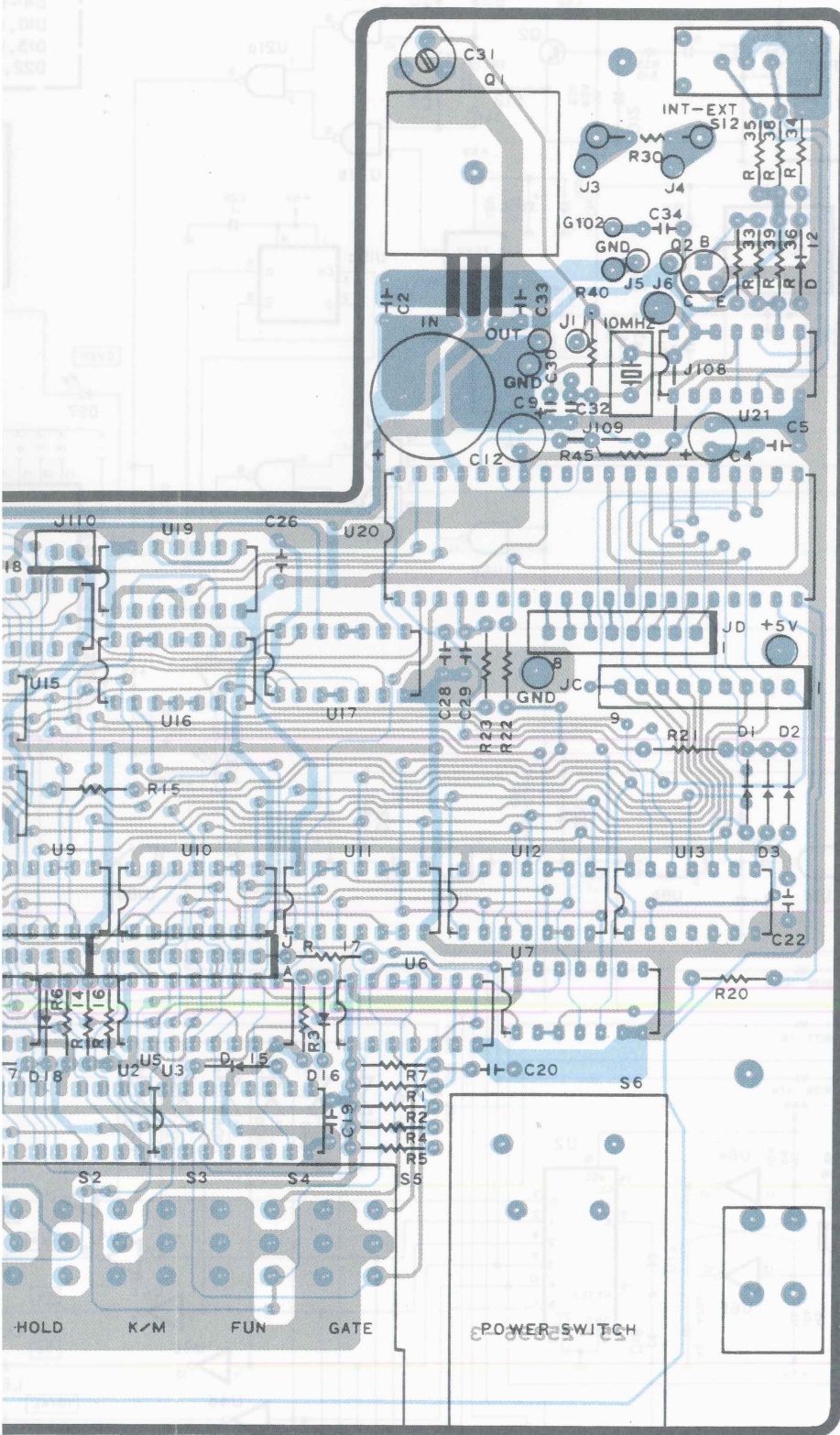


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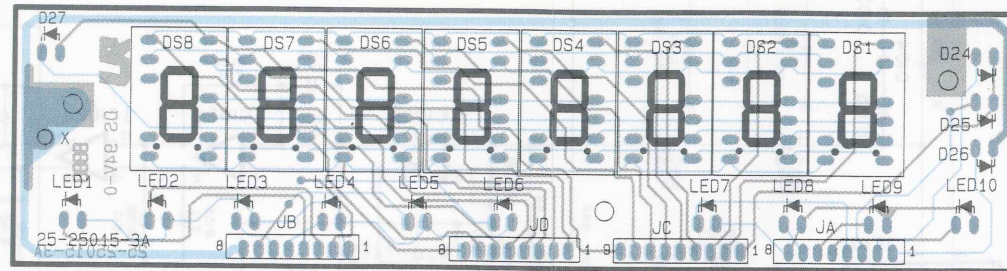




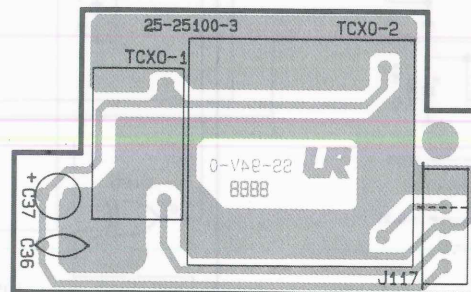
P.C. BOARD



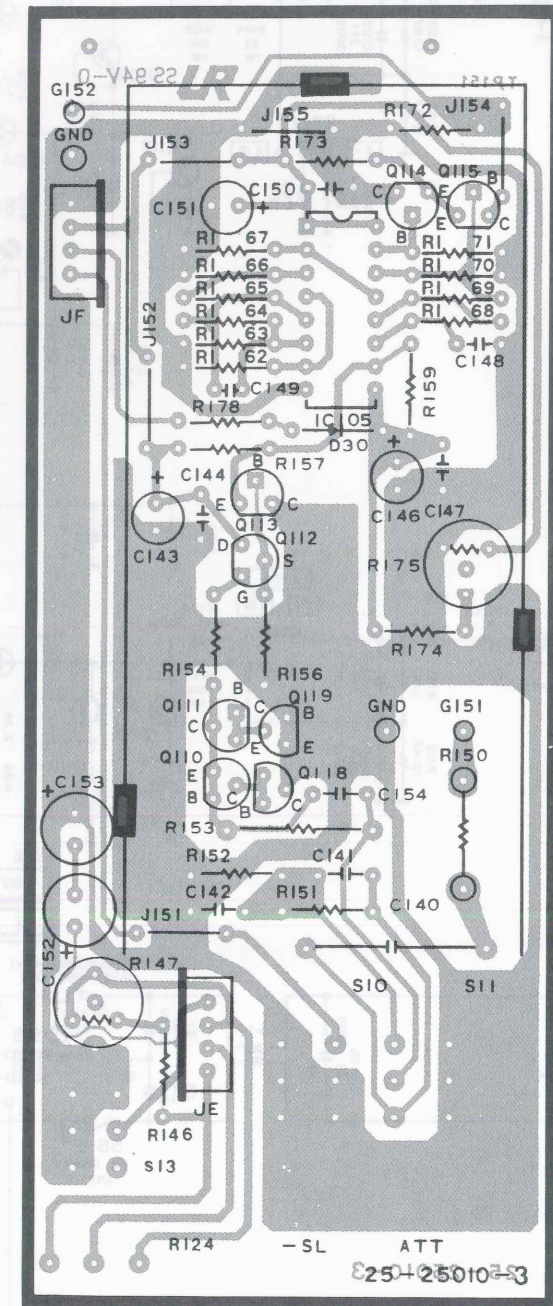
DISPLAY UNIT (W02-0490-08)



TCXO UNIT (W02-0491-08)

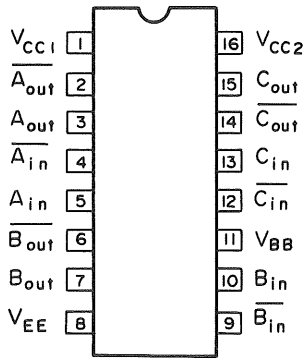


CHANNEL B UNIT (W02-0492-08)

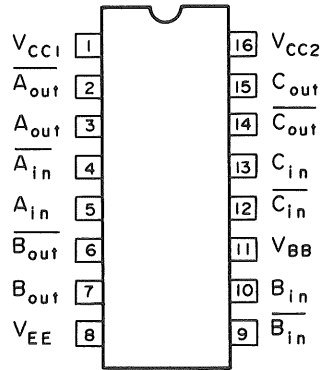




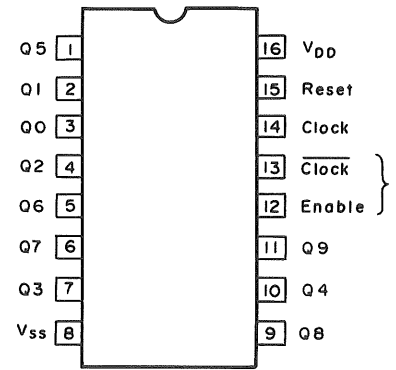
# SEMICONDUCTORS



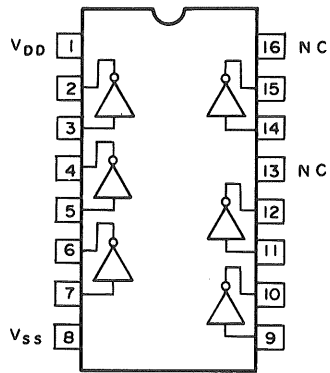
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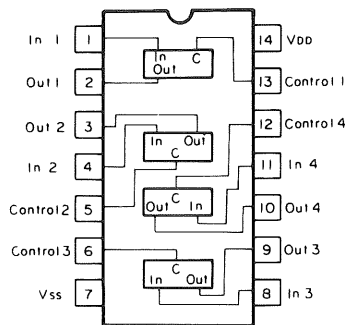
MC10216P



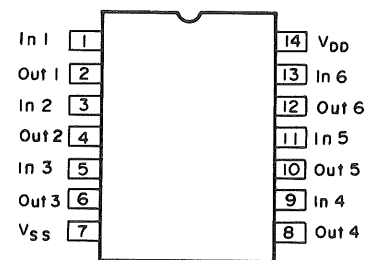
MC14017BCP  
HD14017BD



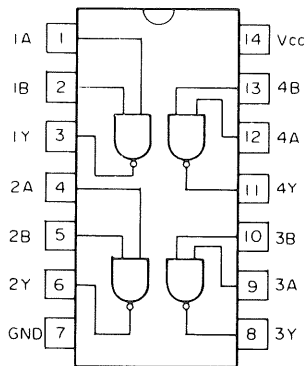
MC14049uBCP



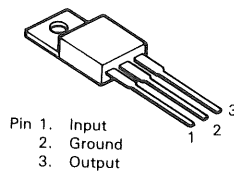
MC14066BCP  
HD14066BP



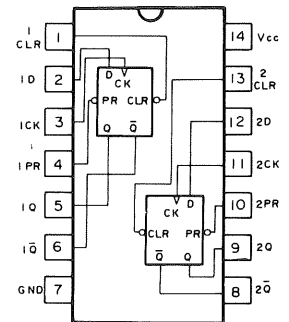
MC14069BCP



MC74HC00  
SN74SOON  
SN74LSOON  
CD74HCT00  
HD74LSOOP

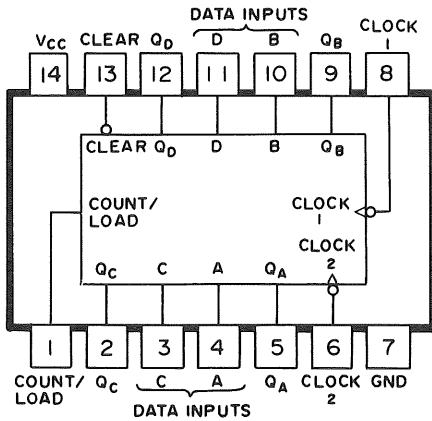


MC7805CT

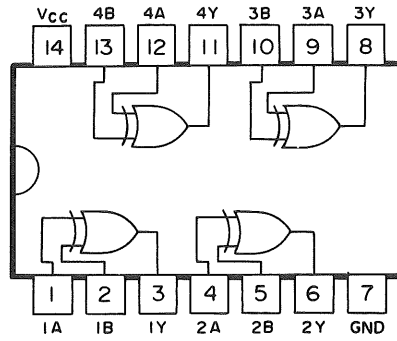


SN74ALS74AN

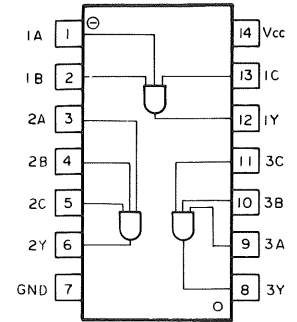
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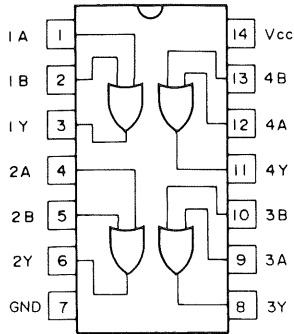
SN74S196



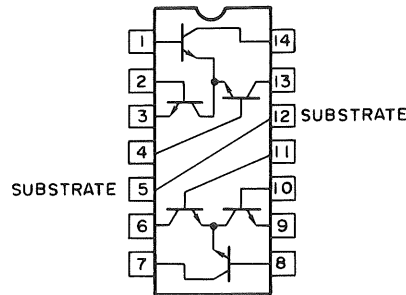
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HD74LS86P



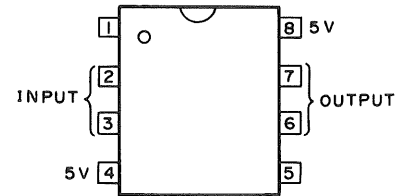
HD74LS11P



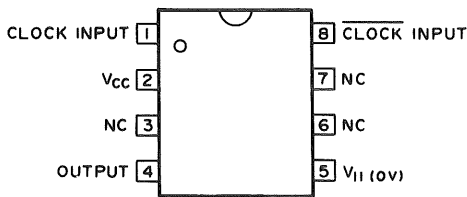
HD74LS32P



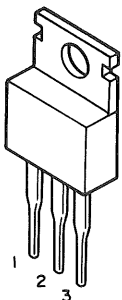
CA3102E



SP4660

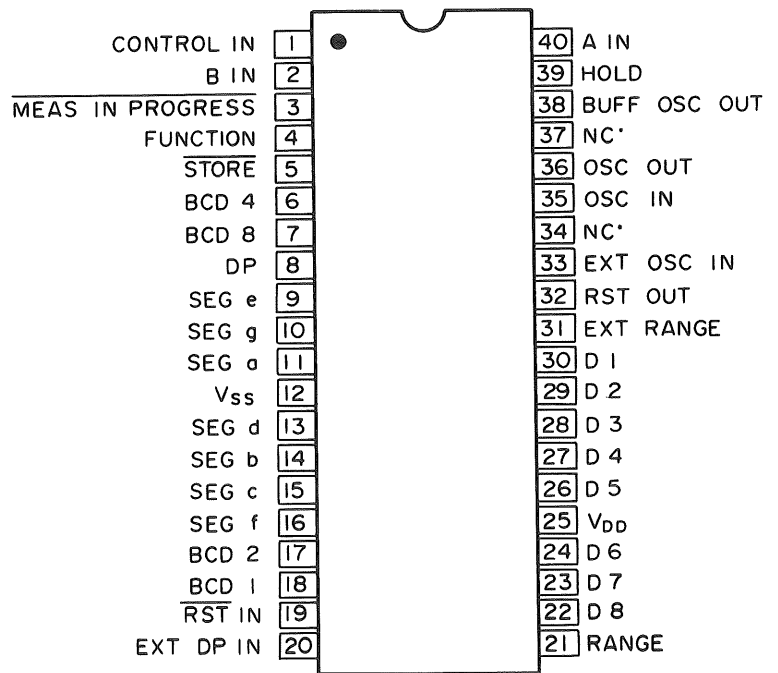


SP8660



- 1. Input
- 2. Ground
- 3. Output

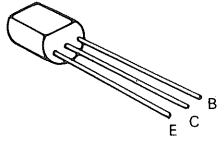
HA17805P



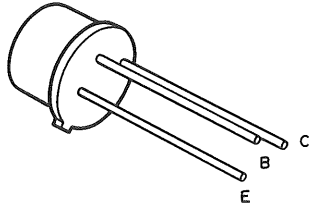
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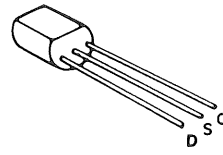
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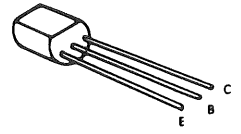
2SC535C  
2SC1674(K)  
2SC1815(GR)



2N2369



2N5486



MPS3640

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A product of  
**KENWOOD CORPORATION**  
17-5, 2-chome, Shibuya, Shibuya-ku, Tokyo 150, Japan

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